PGA309

Voltage Output Programmable Sensor Conditioner

User's Guide

Literature Number: SBOU024B
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This user's guide describes the function and operation of the PGA309.

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Introduction

This user's guide describes the function and operation of the PGA309, a programmable analog signal conditioner designed for bridge sensors.

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1.1 PGA309 Functional Description

The PGA309 is a smart programmable analog signal conditioner designed for resistive bridge sensor applications. It is a complete signal conditioner with bridge excitation, initial span and offset adjustment, temperature adjustment of span and offset, internal/external temperature measurement capability, output over-scale and under-scale limiting, fault detection, and digital calibration. The PGA309, in a calibrated sensor module, can reduce errors to the level approaching the bridge sensor repeatability. Figure 1-1 shows a block diagram of the PGA309. Following is a brief overview of each major function.

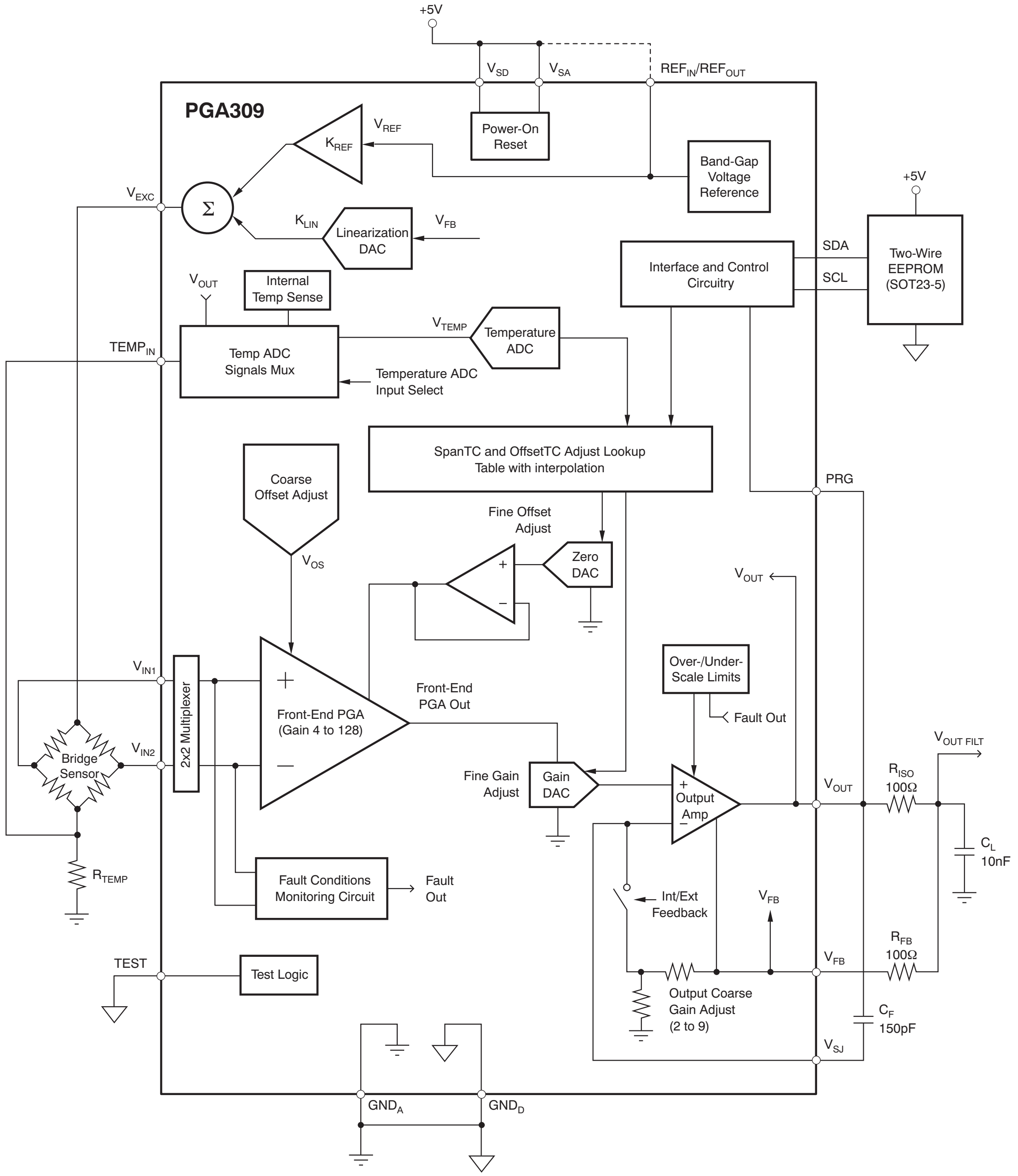

Figure 1-1. Simplified Diagram of the PGA309

1.2 Sensor Error Adjustment Range

The adjustment capability of the PGA309 is summarized in Table 1-1.

Table 1-1. PGA309 Adjustment Capability

Parameter	Value/Range
FSS (full-scale bridge sensitivity)	1mV/V to 245mV/V
Span TC	Over ±3300ppmFS/°C (1)
Span TC nonlinearity	> 10%
Zero offset	±200%FS (2)
Zero offset TC	Over ±3000ppmFS/°C (2)
Zero offset TC nonlinearity	> 10%
Sensor impedance	Down to 200Ω (3)

(1) Depends on the temperature sensing scheme.

(2) Combined coarse and fine offset adjust.

(3) Lower impedance possible by using a dropping resistor in series with the bridge.

1.3 Gain Scaling

The core of the PGA309 is the precision low-drift and no 1/f noise Front-End Programmable Gain Amplifier (Front-End PGA). The overall gain of the Front-End PGA + Output Amplifier can be adjusted from 2.7V/V to 1152V/V. The polarity of the inputs can be switched through the 2x2 input mux to accommodate sensors with unknown polarity output.

The Front-End PGA provides initial coarse signal gain using a no 1/f noise, auto-zero instrumentation amplifier. The fine gain adjust is accomplished by the 16-bit attenuating Gain Digital-to-Analog Converter (Gain DAC). The Gain DAC is controlled by the data in the Temperature Compensation Lookup Table driven by the Temperature Analog-to-Digital Converter (Temp ADC). In order to compensate for second-order and higher drift nonlinearity, the span drift can be fitted to piecewise linear curves during calibration with the coefficients stored in an external nonvolatile EEPROM lookup table.

Following the fine gain adjust stage is the Output Amplifier that provides additional programmable gain. Two key Output Amplifier connections, V_{FB} and V_{SJ}, are brought out on the PGA309 for application flexibility. These connections allow for an accurate conditioned signal voltage while also providing a means for PGA309 output overvoltage and large capacitive loading for RFI/ EMI filtering required in many end applications.

1.4 Offset Adjustment

The sensor offset adjustment is performed in two stages. The input referred Coarse Offset Adjust DAC has approximately a ±60mV offset adjustment range for a selected V_{REF} of 5V. The fine offset and the offset drift are canceled by the 16-bit Zero DAC that sums the signal with the output of the Front-End PGA. Similar to the Gain DAC, the input digital values of the Zero DAC are controlled by the data in the Temperature Compensation Lookup Table, stored in external EEPROM, driven by the Temp ADC. The programming range of the Zero DAC is 0 to V_{REF}, with an output range of 0.1V to $V_{SA} - 0.1V$.

1.5 Voltage Reference

The PGA309 contains a precision low-drift voltage reference (selectable for 2.5V or 4.096V) that can be used for external circuitry through the REF_{IN}/REF_{OUT} pin. This same reference is used for the Coarse Offset Adjust DAC, Zero DAC, Over/Under-Scale Limits and sensor excitation/linearization through the V_{EXC} pin. When the internal reference is disabled, the REF_{IN}/REF_{OUT} pin should be connected to an external reference or to V_{SA} for ratiometric-scaled systems.

1.6 Sensor Excitation and Linearization

A dedicated circuit with a 7-bit + sign DAC for sensor voltage excitation and linearization is provided on the PGA309. This block scales the reference voltage and sums it with a portion of the PGA309 output to compensate the positive or negative bow-shaped nonlinearity exhibited by many sensors over their applied pressure range. Sensors not requiring linearization can be connected directly to the supply (V_{SA}) or to the V_{EXC} pin with the Linearization DAC (Lin DAC) set to zero.

1.7 ADC for Temperature Sensing

The compensation for the sensor span and offset drifts is driven by the temperature sense circuitry. Either internal or external temperature sensing is possible. The temperature can be sensed in one of the following ways:

- Bridge impedance change (excitation current sense, in the positive or negative part of the bridge), for sensors with large temperature coefficient of resistance (TCR > 0.1%/°C)
- On-chip PGA309 temperature, when the chip is located sufficiently close to the sensor
- External diode, thermistor, or RTD placed on the sensor membrane. An internal 7μA current source may be register-enabled to excite these types of temperature sensors.

The temperature signal is digitized by the onboard Temp ADC. The output of the Temp ADC is used by the control digital circuit to read data from the Lookup Table in an external EEPROM, and set the output of the Gain DAC and the Zero DAC to the calibrated values as temperature changes.

An additional function provided through the Temp ADC is the ability to read the V_{OUT} pin back through the Temp ADC input mux. This provides flexibility for a digital output through either One-Wire or Two-Wire interface, as well as the possibility for an external microcontroller to perform real-time custom calibration of the PGA309.

1.8 External EEPROM and Temperature Coefficients

The PGA309 uses an industry-standard Two-Wire external EEPROM (typically, a SOT23-5 package). A 1k-bit (minimum) EEPROM is needed when using all 17 temperature coefficients. Larger EEPROMs may be used to provide user space for serial number, lot code, or other data.

The first part of the external EEPROM contains the configuration data for the PGA309, with settings for:

- Register 3—Reference Control and Linearization
- Register 4—PGA Coarse Offset and Gain/Output Amplifier Gain
- Register 5—PGA Configuration and Over/Under-Scale Limit
- Register 6—Temp ADC Control

This section of the EEPROM contains its own individual checksum (Checksum1).

The second part of the external EEPROM contains up to 17 temperature index values and corresponding temperature coefficients for the Zero DAC and Gain DAC adjustments with measured temperature and contains its own checksum (Checksum2). The PGA309 lookup logic contains a linear interpolation algorithm for accurate DAC adjustments between stored temperature indexes. This approach allows for a piecewise linear temperature compensation of up to 17 temperature indexes and associated temperature coefficients.

If either Checksum1, Checksum2, or both are incorrect, the output of the PGA309 is set to high-impedance.

1.9 Fault Monitor

To detect sensor burnout or a short-circuit, a set of four comparators are connected to the inputs of the Front-End PGA. If any of the inputs are taken to within 100mV of ground or V_{EXC}, or violate the input CMR of the Front-End PGA, then the corresponding comparator sets a sensor fault flag that causes the PGA309 V_{OUT} to be driven within 100mV of either V_{SA} or ground, depending upon the alarm configuration setting (Register 5—PGA Configuration and Over/Under-Scale Limit). This will be well above the set over-scale limit level or well below the set under-scale limit level. The state of the fault condition can be read in digital form in Register 8—Alarm Status Register. If the Over/Under-Scale Limit is disabled, the PGA309 output voltage will still be driven within 100mV of either V_{SA} or ground, depending upon the alarm configuration setting.

There are five other fault detect comparators that help detect subtle PGA309 front-end violations that could otherwise result in linear voltages at V_{OUT} that would be interpreted as valid states. These are especially useful during factory calibration and setup and are configured through Register 5—PGA Configuration and Over/Under-Scale Limit. Their status can also be read back through Register 8—Alarm Status Register.

1.10 Over-Scale and Under-Scale Limits

The over-scale and under-scale limit circuitry combined with the fault monitor circuitry provides a means for system diagnostics. A typical sensor-conditioned output may be scaled for 10% to 90% of the system ADC range for the sensor normal operating range. If the conditioned pressure sensor is below 4%, it is considered under-pressure; if over 96%, it is considered over-pressure.

The PGA309 over/under-scale limit circuit can be programmed individually for under-scale and over-scale that clip or limit the PGA309 output. From a system diagnostic view, 10% to 90% of ADC range is normal operation, < 4% is under-pressure, and > 96% is over-pressure. If the fault detect circuitry is used, a detected fault will cause the PGA309 output to be driven to positive or negative saturation. If this fault flag is programmed for high, then > 97% ADC range will be a fault; if programmed for low, then < 3% ADC range will be a fault. Now the system software can be used to distinguish between over- or under-pressure condition, which indicates an out-of-control process, or a sensor fault.

1.11 Power-Up and Normal Operation

The PGA309 has circuitry to detect when the power supply is applied to the PGA309, and reset the internal registers and circuitry to an initial state. This reset also occurs when the supply is detected to be invalid, so that the PGA309 is in a known state when the supply becomes valid again. The rising threshold for this circuit is typically 2.2V and the falling threshold is typically 1.7V. After the power supply becomes valid, the PGA309 waits for approximately 33ms and then attempts to read the configuration data from the external EEPROM device.

If the EEPROM has the proper flag set in address location 0 and 1, then the PGA309 continues reading the EEPROM; otherwise, the PGA309 waits for 1.3 seconds before trying again. If the PGA309 detects no response from the EEPROM, the PGA309 waits for 1.3 seconds and tries again; otherwise, the PGA309 tries to free the bus and waits for 33ms before trying to read the EEPROM again. If successful (including valid checksum data), the PGA309 triggers the Temp ADC to measure temperature. For 16-bit resolution results the converter takes approximately 125ms to complete a conversion. Once the conversion is complete, the PGA309 begins reading the Lookup Table information from the EEPROM to calculate the settings for the Gain DAC and Zero DAC. This process is detailed in the flowchart shown in Figure 3-1.

The PGA309 reads the entire Lookup Table so that it can determine if the checksum for the Lookup Table is correct. Each entry in the Lookup Table requires approximately 500μs to read from the EEPROM. Once the checksum is determined to be valid, the calculated values for the Gain and Zero DACs are updated into their respective registers, and the Output Amplifier is enabled. The PGA309 then begins looping through this entire procedure, starting with reading the EEPROM configuration registers, then starting a new conversion on the Temp ADC, which then triggers reading the Lookup Table data from the EEPROM. This loop continues indefinitely.

1.12 Digital Interface

There are two digital interfaces on the PGA309. The PRG pin uses a One-Wire, UART-compatible interface with bit rates from 4.8Kbits/s to 38.4Kbits/s. The SDA and SCL pins together form an industry standard Two-Wire interface at clock rates from 1kHz to 400kHz. The external EEPROM uses the Two-Wire interface. Communication to the PGA309 internal registers, as well as to the external EEPROM, for programming and readback can be conducted through either digital interface.

It is also possible to connect the One-Wire communication pin, PRG, to the V_{OUT} pin in true three-wire sensor modules and still allow for programming. In this mode, the PGA309 Output Amplifier may be enabled for a set time period and then disabled again to allow sharing of the PRG pin with the V_{OUT} connection. This allows for both digital calibration and analog readback during sensor calibration in a three-wire sensor module.

The Two-Wire interface has timeout mechanisms to prevent bus lockup from occurring. The Two-Wire master controller in the PGA309 has a mode that attempts to free up a stuck-at-zero SDA line by issuing SCL pulses, even when the bus is not indicated as idle after the timeout period has expired. The timeout will only apply when the master portion of the PGA309 is attempting to initiate a Two-Wire communication.

1.13 Pin Configuration

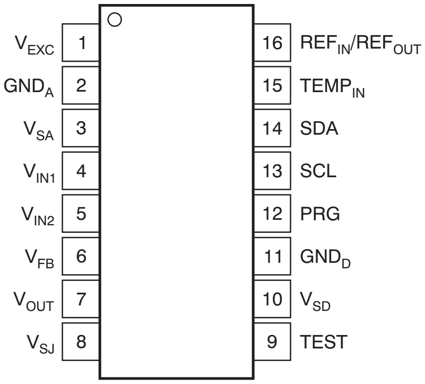

Figure 1-2. PGA309 Pin Assignments

Table 1-2. PGA309 Pin Descriptions

Pin	Name	Description
1	V_{EXC}	Bridge sensor excitation. Connect to bridge if linearization and/or internal reference for bridge excitation is to be used.
2	GND_A	Analog ground. Connect to analog ground return path for V_{SA}. Should be same as GND_D.
3	V_{SA}	Analog voltage supply. Connect to analog voltage supply. To be within 200mV of V_{SD}.
4	V_{IN1}	Signal input voltage 1. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to Front-End PGA.
5	V_{IN2}	Signal input voltage 2. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to Front-End PGA.
6	V_{FB}	V_{OUT} feedback pin. Voltage feedback sense point for over/under-scale limit circuitry. When internal gain set resistors for the Output Amplifier are used, this is also the voltage feedback sense point for the Output Amplifier. V_{FB} in combination with V_{SJ} allows for ease of external filter and protection circuits without degrading the PGA309 V_{OUT} accuracy. V_{FB} must always be connected to either V_{OUT} or the point of feedback for V_{OUT}, if external protection is used.
7	V_{OUT}	Analog output voltage of conditioned sensor.
8	V_{SJ}	Output Amplifier summing junction. Use for Output Amplifier compensation when driving large capacitive loads (> 100pF) and/or for using external gain setting resistors for the Output Amplifier.
9	TEST	Test/External Controller Mode pin. Pull to GND_D in normal mode.
10	V_{SD}	Digital voltage supply. Connect to digital voltage supply. To be within 200mV of V_{SA}.
11	GND_D	Digital ground. Connect to digital ground return path for V_{SD}. Should be same as GND_A.
12	PRG	Single-wire interface program pin. UART-type interface for digital calibration of the PGA309 over a single wire. Can be connected to V_{OUT} for a three-lead (V_S, GND, V_{OUT}) digitally programmable sensor assembly.
13	SCL	Clock input/output for Two-Wire, industry-standard compatible interface for reading and writing digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface.
14	SDA	Data input/output for Two-Wire, industry-standard compatible interface for reading and writing digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface.
15	$TEMP_{IN}$	External temperature signal input. PGA309 can be configured to read a bridge current sense resistor as an indicator of bridge temperature, or an external temperature sensing device such as diode junction, or RTD, or thermistor. This input can be internally gained up by 1, 2, 4, or 8. In addition, this input can be read differentially with respect to V_{GNDA}, V_{EXC}, or the internal V_{REF}. There is also an internal, register-selectable, 7µA current source (I_{TEMP}) that can be connected to $TEMP_{IN}$ as an RTD, thermistor, or diode excitation source.
16	REF_{IN}/REF_{OUT}	Reference input/output pin. As an output, the internal voltage reference (selectable as 2.5V or 4.096V) is avail-able for system use on this pin. As an input, the internal voltage reference may be disabled and an external voltage reference can then be applied as the reference for the PGA309.

Chapter 2

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Detailed Description

This chapter provides a detailed description of the PGA309.

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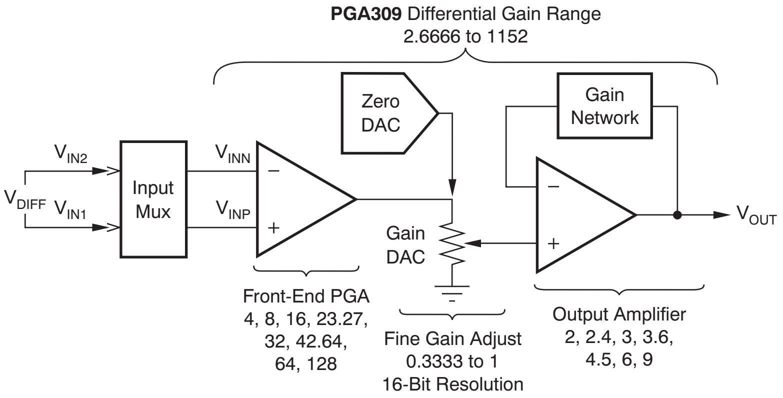
2.1 Gain Scaling

The PGA309 contains three main gain blocks for scaling differential input bridge sensor signals, as shown in Figure 2-1. The Front-End PGA contains the highest gain selection to allow for the highest signal-to-noise ratio by applying the largest gain at the front of the signal chain before the addition of other noise sources. The Front-End PGA gain select has eight gain settings (4, 8, 16, 23.27, 32, 42.67, 64, and 128) and is set by Register 4 bits (11:8). Bit 11 selects the polarity of the input mux.



NOTE: V_{OUT} = [(V_{DIFF} + $V_{COARSE\ OFFSET}$)(Front-End PGA Gain) + $V_{ZERO\ DAC}$][Gain DAC][Output Amplifier Gain]

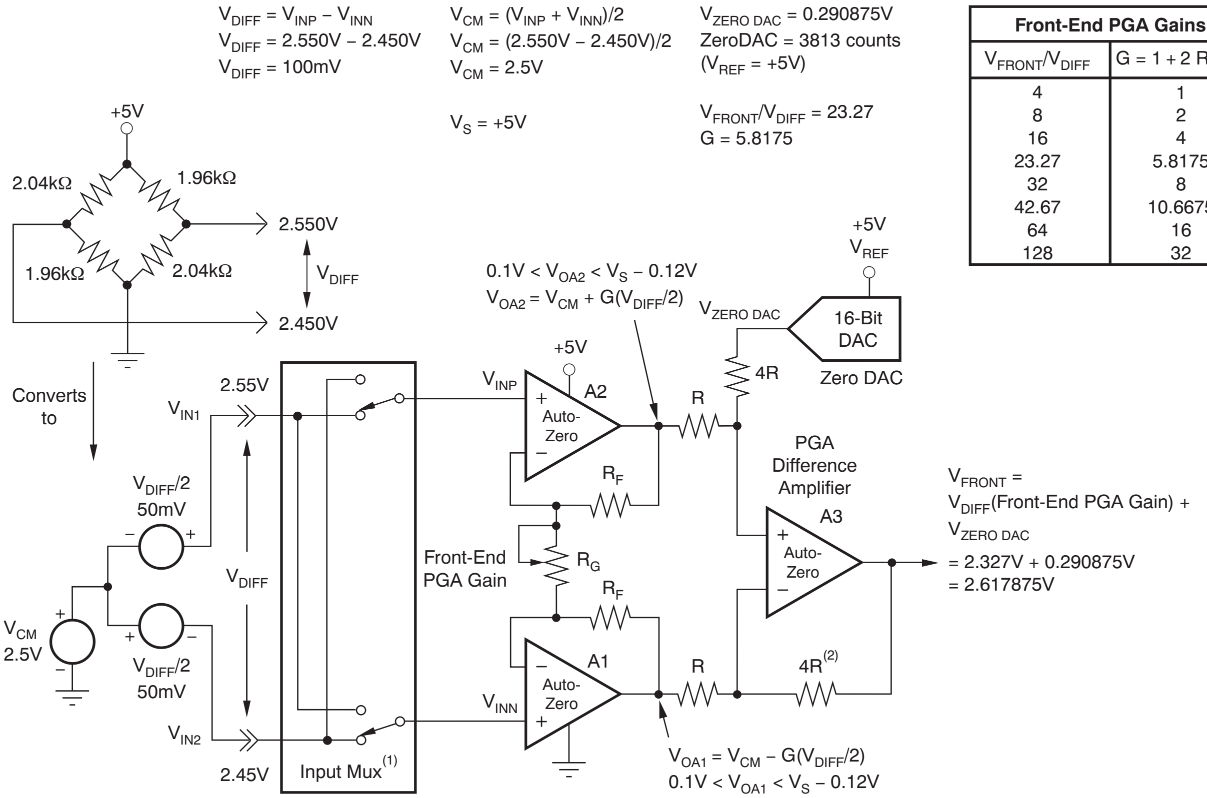
Figure 2-1. Gain Blocks of the PGA309

The Front-End PGA is followed by the Gain DAC. The fine gain adjust is controlled by the 16-bit Gain DAC and is adjustable from 0.3333 to 1. Register 2 is used only for the Gain DAC setting.

Final signal gain is applied through the Output Amplifier, which has an internal select of seven gain settings (2, 2.4, 3, 3.6, 4.5, 6, 9). The Output Amplifier has a selection to disable the internal gain and allow user-supplied external resistors to set the Output Amplifier gain. Register 4 bits (14:12) select the internal Output Amplifier gains, except when programmed with ‘111’ when the internal feedback is disabled. The combined gain blocks allow for a V_{OUT}/V_{DIFF} signal gain of 2.666 (400kHz bandwidth) to 1152 (60kHz bandwidth).

The Front-End PGA of the PGA309 is a three op amp instrumentation amplifier for optimum rejection of common-mode voltages. This instrumentation amplifier is constructed using op amps with auto-zero front-ends to virtually eliminate 1/f noise.

As with any instrumentation amplifier, there are limitations on the output voltage swing and input common-mode voltage range. The circuit in Figure 2-2 is representative of the Front-End PGA inside of the PGA309 and is used to evaluate critical internal node voltages to ensure that output voltage swing and common-mode limits are not violated. It is possible to violate the limits of these internal nodes and still have apparently valid output voltages at V_{OUT} of the PGA309. There are internal comparators that can be set to monitor these internal nodes to indicate an out-of-limit condition during sensor calibration (see Section 2.8, *Fault Monitor*).



Front-End PGA Gains	
V_{FRONT}/V_{DIFF}	$G = 1 + 2\ R_F/R_G$
4	1
8	2
16	4
23.27	5.8175
32	8
42.67	10.6675
64	16
128	32

(1) Input mux allows for sensor output polarity reversal.

(2) PGA difference amplifier gain of 4 allows full range out of Zero DAC and full voltage swing out of A1 and A2 without common-mode violation on A3 input.

Figure 2-2. Front-End PGA Gain—Internal Node Calculations

After choosing appropriate scaling for the PGA309 gain blocks, a simple hand analysis can check for internal node limit violations. It is important to convert the PGA309 input voltages (V_{INP}, V_{INN}) to common-mode and differential components for the maximum sensor output. The model for this conversion is illustrated in Figure 2-2. The Front-End PGA has a gain of 4 in difference amplifier A3. To analyze important internal nodes V_{OA1} and V_{OA2}, it is necessary to assign the proper gain factor (G) to op amps A1 and A2. This is detailed in Figure 2-2 with the respective equations for the output voltages shown at the appropriate nodes. For maximum V_{DIFF} output of the sensor, V_{OA1} and V_{OA2} are within the allowed voltage swing of: $0.1V < (V_{OA1}$ or $V_{OA2}) < V_S - 0.12$. Or, for this example: $0.1V < (V_{OA1}$ or $V_{OA2}) < 4.88V$.

Other applications may yield different results that require different gain scaling or a resistor in the positive or negative leg of the sensor excitation path to adjust the common-mode input voltage of the PGA309. The maximum allowable input voltage range (IVR) of the PGA309 is specified as $0.2V < IVR < V_{SA} - 1.5V$, which for this application translates to $0.2V < IVR < 3.5V$. In Figure 2-2 we see $V_{INP} = 2.550V$ and $V_{INN} = 2.450V$, which is within the acceptable IVR specification.

The output (V_{FRONT}) of difference amplifier A3 has a gain of 4 in it for voltages out of A2 and A1, but a gain of 1 for voltages out of the Zero DAC. V_{FRONT} is shown with the contribution from V_{DIFF} times the Front-End PGA gain plus the Zero DAC output voltage. The V_{FRONT} signal is further processed through the Gain DAC and Output Amplifier gain blocks.

Figure 2-3 depicts the Gain DAC and Output Amplifier gain blocks inside the PGA309. For this example the Gain DAC was set to 0.859475571 and the Output Amplifer to a gain of 2. As shown in Figure 2-3, the net output voltage, V_{OUT}, is 4.5V for the maximum V_{DIFF} output of the sensor.

For $V_{OUT\ MIN}$, the sensor output of 0V:

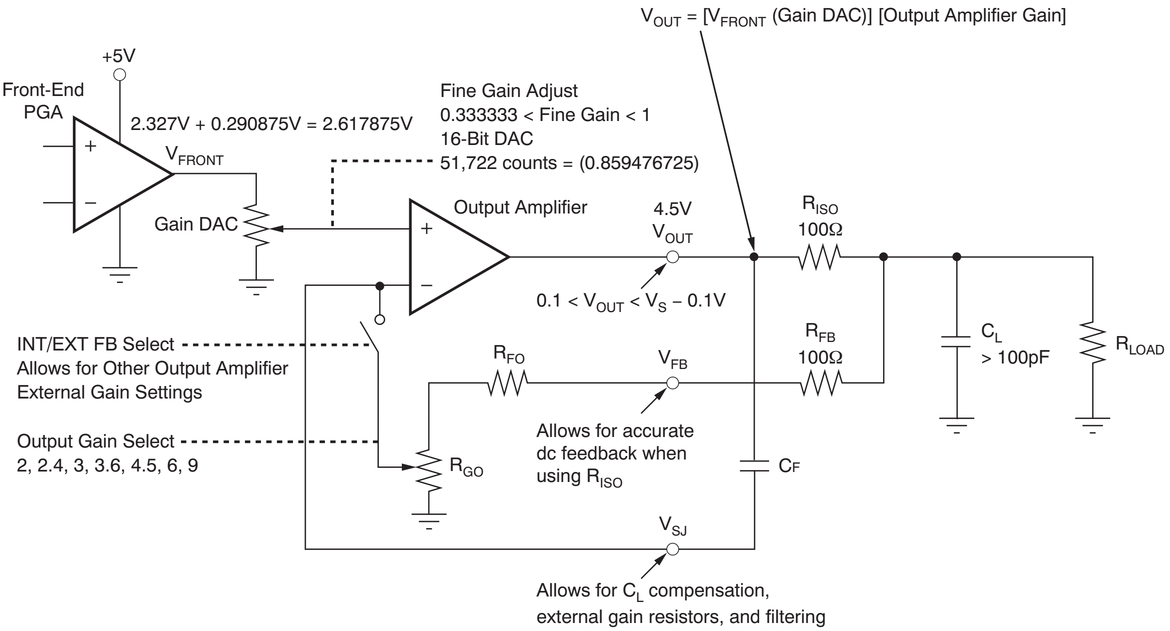
$V_{OUT\ MIN} = V_{ZERO\ DAC}$ [(Gain DAC)(Output Amplifier Gain)]

For this example:

$V_{OUT\ MIN} = 0.290908813V\ [(0.859475571)(2)] = 0.5000V$

The Output Amplifier has external connections, which allow the end-user maximum flexibility in Output Amplifier configurations for a variety of applications. The use of the V_{FB} and V_{SJ} pins, are described in Section 2.4, *Output Amplifier*.

Example 2-1 shows the procedure for solving for gain settings.



NOTE: $V_{OUT} = [(V_{DIFF} + V_{COARSE\ OFFSET})$(Front-End PGA Gain) + $V_{ZERO\ DAC}$][Gain DAC][Output Amplifier Gain]

Figure 2-3. Fine Gain Adjust of the PGA309

2.1.1 *PGA309 Transfer Function*

Equation 1 shows the mathematical expression that is used to compute the output voltage, V_{OUT}. This equation can also be rearranged algebraically to solve for different terms. For example, during calibration, this equation is rearranged to solve for V_{IN}.

$$V_{OUT} = \left[\left(\text{mux\_sign} \bullet V_{IN} + V_{Coarse\_Offset}\right) \bullet GI + V_{Zero\_DAC}\right] \bullet GD \bullet GO \qquad (1)$$

Where:

mux_sign: This term changes the polarity of the input signal; value is ±1.
V_{IN}: The input signal for the PGA309; $V_{IN}1 = V_{INP}$, $V_{IN}2 = V_{INN}$.
V_{Coarse_Offset}: The coarse offset DAC output voltage.
GI: Input stage gain.
V_{Zero_DAC}: Zero DAC output voltage.
GD: Gain DAC.
GO: Output stage gain.

Example 2-1. Solving For Gain Settings

An example bridge sensor application will be used to examine internal nodes of the PGA309 that are related to the gain blocks (refer to Figure 2-2 and Figure 2-3).

Given:

Full-Scale Bridge Sensitivity (FSS) = 20mV/V (sensor span)
V_{OS} = 0mV (sensor offset)
V_{REF} = +5V (sensor excitation)
V_B = +5V, VS = +5V
R_{BRG} = 2kΩ
$V_{OUT\ MIN}$ = +0.5V
$V_{OUT\ MAX}$= +4.5V

Find:

Front-End PGA Gain
Gain DAC Setting
Zero DAC Setting
Output Amplifier Gain

Solution:

1. Maximum Sensor Output:
   $V_{BRmax} = (FSS)(V_B)$
   $V_{BRmax} = (20mV/V)(5V)$
   $V_{BRmax} = 100mV$
2. Total Desired Gain:
   $G_T = (V_{OUT\ MAX} - V_{OUT\ MIN})/V_{BRmax}$
   $G_T = (4.5V - 0.5V)/100mV$
   $G_T = 40$
3. Partition the Gain; Determine the Desired Gain DAC Setting:
   Choose Front-End PGA Gain = 23.27
   Choose Output Amplifier Gain = 2
   Gain DAC = 0.859475719
   Gain DAC = G_T/[(Front-End PGA)(Output Amplifier Gain)]
   Gain DAC = 40/[(23.27)(2)]
   Gain DAC = 0.859475719
4. Calculate exact programmable Gain DAC value:
   Decimal # counts = (Gain DAC − 1/3)(3/2)(65536)
   Decimal # counts = (0.859475719 − 1/3)(3/2)(65536) = 51,721.90133
   Use 51,722 counts→CA0Ah→1100 1010 0000 1010 →0.859476725
   Gain DAC = (# counts/65536)(2/3)+(1/3)
5. Calculate Zero DAC value
   $V_{ZERO\ DAC} = V_{OUT\ MIN}$/[(Gain DAC)(Output Amplifier Gain)]
   $V_{ZERO\ DAC}$ = 0.5V/[(0.859475571)(2)] = 0.29087505V
   Decimal # counts = $V_{ZERO\ DAC}/(V_{REF}/65536)$
   Decimal # counts = 0.29087505/(5/65536) = 3812.55746
   Use 3813 counts→0EE5h→0000 1110 1110 0101 →0.290908813V
   $VZ_{ERO\ DAC}$ = (# counts/65536)(V_{REF})
6. Calculate V_{CM} and V_{DIFF} for Maximum Sensor Output (see Figure 2-2): $V_{DIFF} = V_{INP} - V_{INN}$
   $V_{DIFF} = 2.550 - 2.450$
   $V_{DIFF} = 100mV$; $V_{DIFF}/2 = 50mV$
   $V_{CM} = (V_{INP} + V_{INN})/2$
   $V_{CM} = (2.550V + 2.450V)/2$
   $V_{CM} = 2.5V$
7. Check Internal Nodes V_{OA2} and V_{OA1}: Front-End PGA Gain = 23.27
   G = 5.8175 (see Figure 2-2)
   $V_{OA1} = V_{CM} - G(V_{DIFF}/2)$
   $V_{OA1} = 2.5V - 5.8175(50mV)$
   $V_{OA1} = 2.209125$

Example 2-1. Solving For Gain Settings (continued)

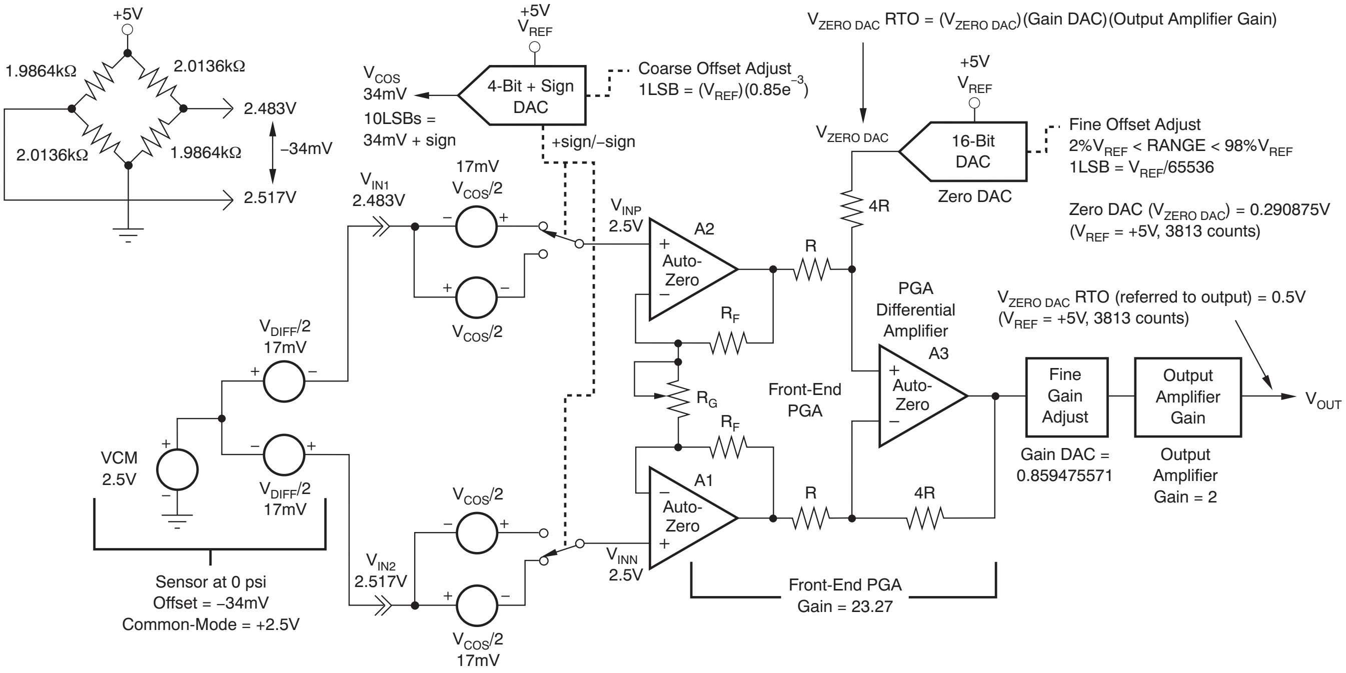
$V_{OA2} = V_{CM} + G(V_{DIFF}/2)$
$V_{OA2} = 2.5V + 5.8175(50mV)$
$V_{OA2} = 2.790875$
$0.1V \le V_{OA1}$ and $V_{OA2} \le V_S - 0.12V$
$0.1V \le V_{OA1}$ and $V_{OA2} \le 4.88V$
Therefore, V_{OA1} and V_{OA2} are valid.

8. Check Internal Nodes V_{OA3} (V_{FRONT}):
   $V_{FRONT} = V_{DIFF}$ (Front-End PGA Gain) + $V_{ZERO\ DAC}$
   $V_{DIFF\ MIN} = 0V$
   $V_{DIFF\ MAX} = 100mV$
   Front-End PGA Gain = 23.27
   $V_{ZERO\ DAC} = 0.290908813V$
   $V_{FRONT\ MIN} = (0)(23.27) + 0.290908813V = 0.290908813V$
   $V_{FRONT\ MAX} = (100mV)(23.27) + 0.290908813V = 2.6179V$
   $0.05V < V_{FRONT\ MIN}$ and $V_{FRONT\ MAX} < V_{SA} - 0.1V$
   $0.05V < 0.290908813V$ and $2.6179V < V_{SA} - 0.1V$
   V_{FRONT} OK!

2.2 Offset Scaling

The coarse offset adjust is implemented before the Front-End PGA gain to allow for maximum dynamic range. Many bridge sensors have initial offsets comparable to their maximum scale outputs. The coarse offset adjust can be applied as positive or negative. It is implemented in a 4-bit DAC + sign and contains 14 positive selections, 14 negative selections, and zero.

The resolution in either the positive or negative range is $V_{REF}/1200$. For a +5V reference, this translates to 4.2mV steps. Figure 2-4 depicts the PGA309 with the gain settings used for the example bridge sensor application detailed in Section 2.1, *Gain Scaling*.



NOTE: $V_{OUT} = [(V_{DIFF} + V_{COARSE\ OFFSET})$(Front-End PGA Gain) + $V_{ZERO\ DAC}$][Gain DAC][Output Amplifier Gain]

Figure 2-4. Coarse and Fine Offset Adjust

The conversion of the bridge initial differential offset plus its common-mode to the differential plus common-mode voltage source model is shown in Figure 2-4 for an initial bridge sensor offset of −34mV (V_{INP} – V_{INN}). Conceptually, this divides into two 17mV offset voltages with polarities as shown. If the coarse offset adjust is set for +34mV offset (V_{INP} – V_{INN}), then the initial bridge offset is cancelled exactly. Any residual initial bridge offset not cancelled by the coarse offset adjust will be gained up by the Front-End PGA gain and needs to be accounted for when setting the fine offset adjust by using the Zero DAC.

The coarse offset adjust is set by Register 4 bits (4:0), with bit 4 determining the coarse offset polarity as negative for a ‘1’ and positive for a ‘0’. The internal architecture of the coarse offset adjust does yield duplicate digital codes for both $-7(V_{REF})(0.85e^{-3})$ and $+7(V_{REF})(0.85e^{-3})$. See Section 6.2.5, *Register 4*, for a complete mapping of the coarse offset adjust settings.

The fine offset adjust is set by the Zero DAC. The Zero DAC setting is gained by the Gain DAC and the Output Amplifier gain and is referred-to-output (RTO). The Zero DAC is a unipolar, 16-bit DAC, with its reference being the V_{REF} setting of the PGA309. The range of the Zero DAC is ensured to be linear from 2%V_{REF} to 98%V_{REF}, for V_{REF} = +5V (for V_{REF} < +5V, the upper end of the Zero DAC range can extend to V_{REF}). The Zero DAC analog range is 0.1V ≤ Zero DAC analog range ≤ (V_{SA} − 0.1V). The Zero DAC programming range is 0V ≤ Zero DAC programming range ≤ V_{REF}. The data format is 16-bit unsigned. Register 1 bits (15:0) are used for the Zero DAC setting.

2.3 Zero DAC and Gain DAC Architecture

Two 16-bit DACs are incorporated into the PGA309 for fine adjustment of the Zero DAC and Gain DAC. These DACs are based on a Resistor String (R-String) architecture with very low integral and differential nonlinearities.

The Zero DAC incorporates a buffer amplifier in a gain of 2V/V. The DAC resistor string is connected between the REF_{IN}/REF_{OUT} (V_{REF} voltage) pins and GND_A. The input digital value adjusts the point on the resistor string where the noninverting amplifier input is connected between 0 × V_{REF} to 0.5 × V_{REF}, thus adjusting the Zero DAC output voltage from 0V to V_{REF}. Due to the device output saturation of the buffer amplifier, the linearity of the Zero DAC is specified from 2% to 98% of the digital scale with $V_{REF} = V_{SA}$. However, for cases when $V_{REF} < V_{SA}$ (for example, when using the PGA309 internal reference), the Zero DAC is linear to 100% of full-scale.

The Gain DAC uses a similar R-String architecture. However, the Output Amplifier is performing the function of the buffer amplifier. The R-String of the DAC is connected between the output of the Front-End PGA, V_{FRONT}, and GND_A (see Figure 2-3). The input digital value adjusts the value of the noninverting amplifier input between 1/3 × V_{FRONT} to 1 × V_{FRONT}, thus setting the attenuation factor of the Gain DAC from 0.333V/V to 1V/V with 16-bit precision.

The output of both the Zero and Gain DACs are calculated and adjusted on every Temp ADC measurement according to the Lookup Table stored in EEPROM (see Section 3.2, *EEPROM Content and Lookup Table Calculation*). This leads to DAC code adjustments on small temperature changes. Unlike some string DACs, the proprietary switch architecture of the PGA309 Zero and Gain DACs allows switching with very low glitch energy and essentially no dependency on the code being changed. The glitch energy is normally lower than the voltage noise level at the output of the PGA309.

2.4 Output Amplifier

The Output Amplifier section of the PGA309 is configured to allow maximum flexibility and accuracy in the end application. Figure 2-5 depicts the Output Amplifier in a common three-terminal sensor application. In this application, it is desired to provide overvoltage protection due to mis-wires on the output of the PGA309, as well as a 10nF capacitor on the sensor module output for EMI/RFI filtering. In this configuration, R_{ISO} and R_{FB} provide overvoltage protection on $V_{OUT\ FILT}$ to 16V by limiting the current into V_{OUT} and V_{FB} to about 150mA [(16V − 0.7V)/100Ω]. The 0.7V drop results from the internal ESD structure to GND or V_{SA}. In addition, R_{ISO} serves to isolate the 10nF RFI/ EMI capacitive load from V_{OUT}. R_{FB} adds a slight gain error that is calibrated out with the PGA309 + sensor calibration. Note that the point of feedback around the Output Amplifier is taken from $V_{OUT\ FILT}$ and as such, after PGA309 + sensor calibration, the Output Amplifier will accurately scale $V_{OUTFILT}$ to match the desired conditioned sensor voltage. C_F provides a second feedback path around the Output Amplifier for stability. With the configuration shown, the Output Amplifier is stable for internal Output Amplifier gains from 2 (125kHz bandwidth, 63° loop gain phase margin, typical values) to 9 (64kHz bandwidth, 86° loop gain phase margin, typical values). Table 2-1 details the typical Output Amplifier resistor values for R_{FO} and R_{GO}, as well as open-loop output resistance. These values, combined with the typical Output Amplifier open-loop gain curve and standard op amp stability techniques, allow the Output Amplifier to be tailored and configured for the specific sensor application.

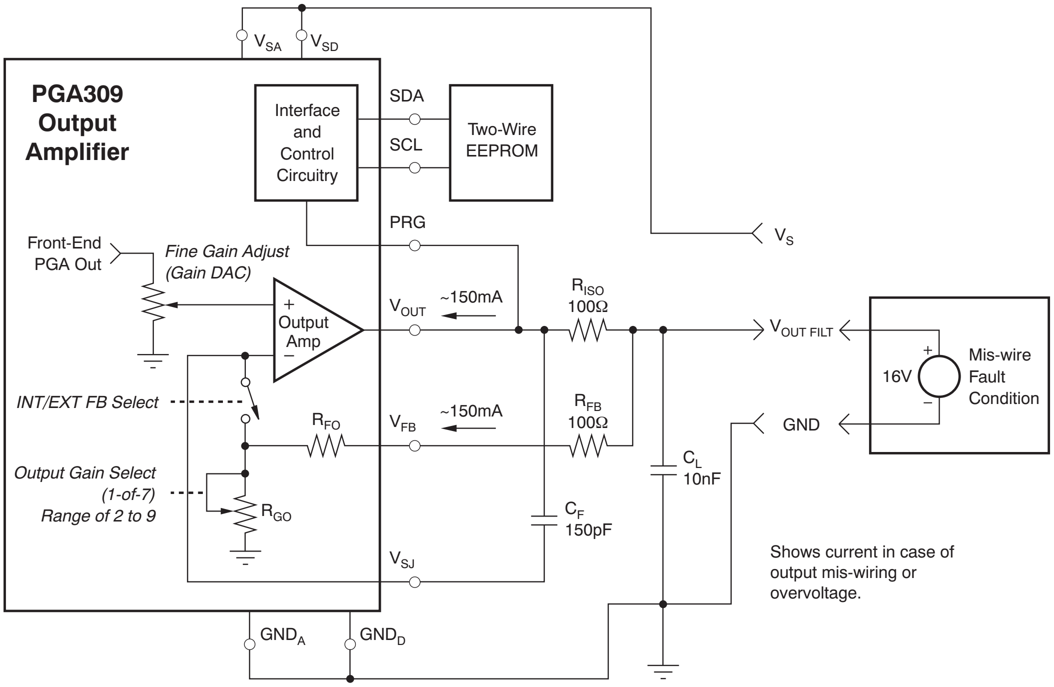


Figure 2-5. Output Amplifier in a Common 3-Terminal Sensor Application

Table 2-1. Output Amplifier Typical Gain Resistor Values(1)

Gain	R_{FO} Typical (kΩ)	R_{GO} Typical (kΩ)
2	18	18
2.4	21	15
3	24	12
3.6	26	10
4.5	28	8
6	30	6
9	32	4

(1) R_O = open-loop output impedance = 675Ω, typical at f = 1MHz, I_{OUT} = 0.

In addition to using its own internal gain setting resistors, R_{FO} and R_{GO}, the Output Amplifier may use external feedback resistors R_{FOEXT} and R_{GOEXT}, as shown in Figure 2-6. Table 2-2 details the bits used in Register 4 for the desired Output Amplifier gain configurations. To use the external feedback resistors, set GO2, GO1, and GO0 to all 1s. In addition to allowing external feedback resistors to be used, this configuration provides a handy mechanism for testing the Output Amplifier stability, even if internal gain settings are to be used. As shown in Figure 2-6, external feedback resistors R_{FOEXT} and R_{GOEXT} are both set to 18kΩ, equivalent to the typical resistor values used for an internal gain setting of 2. If V_{OUT} is biased to mid-scale (+2.5V for V_{SA} = +5V) through the Zero DAC and by setting V_{DIFF} = 0V, a signal generator may be used to inject a 200mV$_{PP}$ square wave (1kHz) into the end of R_{GOEXT} and a response measured at V_{OUT}. This provides a transient response for the Output Amplifier in a given configuration. Standard stability transient response criteria for a dominant two-pole system may be used to determine suitable phase margin based upon the measured overshoot and ringing on V_{OUT}.

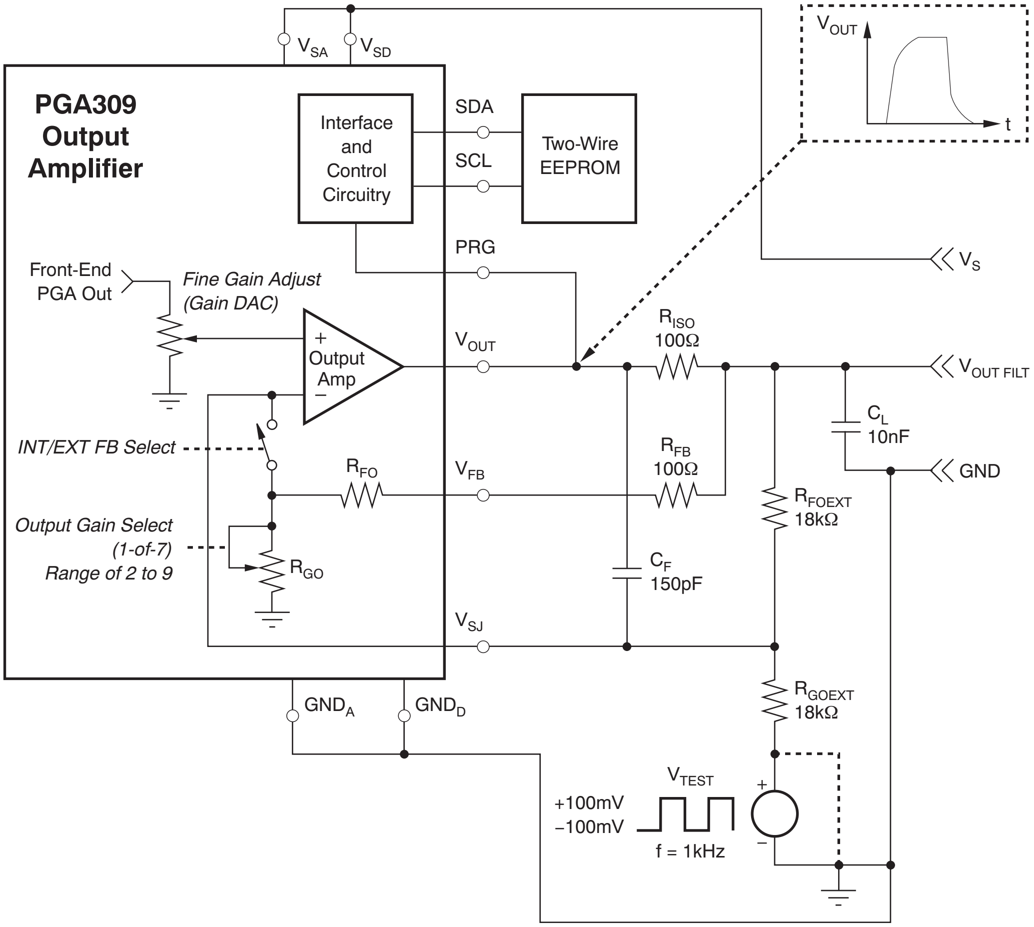
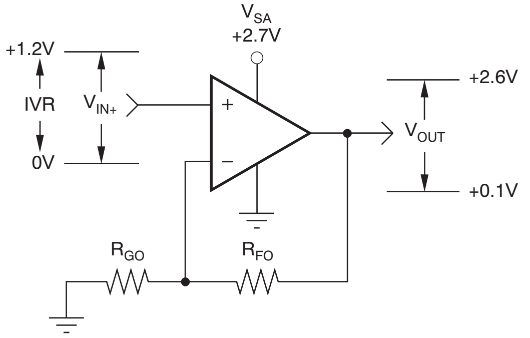


Figure 2-6. Output Amplifier Using External Feedback Resistors R_{FOEXT} and R_{GOEXT}

Table 2-2. Output Amplifier Gain Selections—Register 4

GO2 [14]	GO1 [13]	GO0 [12]	Output Amplifier Gain
0	0	0	2
0	0	1	2.4
0	1	0	3
0	1	1	3.6
1	0	0	4.5
1	0	1	6
1	1	0	9
1	1	1	Disable Internal Feedback

For low-supply applications, the minimum gain for the Output Amplifier is related to its IVR and output voltage swing. In Figure 2-7, the supply is lowered to +2.7V. The tested IVR of the Output Amplifier is 0V to V_{SA}−1.5V, as reflected in Figure 2-7. The output voltage swing is tested to be 0.1V to +2.6V for a 10kΩ load, as shown. This calculates to a minimum gain of 2.08. For best performance, the Output Amplifier should be scaled for a minimum gain of 2.4 for this application. Usually, this is only a factor at lower voltages but is easily checked for each individual application.



Output Amplifier Gain Minimum = V_{OUT}/V_{IN+} = +2.5V/+1.2V = 2.08

Use 2.4

Figure 2-7. Output Amplifier Minimum Gain at Low Supply

2.5 Reference Voltage

The PGA309 can be configured for use with an internal or external voltage reference. The reference voltage is used by the Zero DAC, Over/Under-Scale Limit, Coarse Offset Adjust DAC, Temp ADC, and Bridge Excitation Linearization Circuit. Figure 2-8 depicts the PGA309 reference circuit. If internal reference is selected, either 2.5V or 4.096V can be chosen. In this mode, a typically better than 2% initial accuracy, low drift, ±10ppm/°C reference is available for internal and external use. Up to 5mA can be supplied through the REF_{IN}/REF_{OUT} pin in internal reference mode. If external reference mode is chosen, then an external reference from +2.0V to $+V_{SA}$ may be applied to the REF_{IN}/REF_{OUT} pin. During power-on, the external reference mode is selected. Table 2-3 details the Register 3 bits (9:8) used for the reference mode selections.

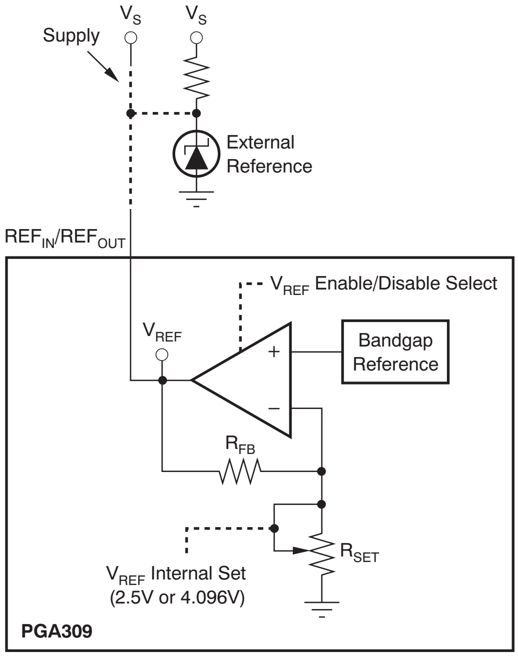


Figure 2-8. PGA309 Reference Circuit

Table 2-3. Register 3 Reference Control Bits

D9	D8		
RS	**REN**	**V_{REF}**	**Reference Configuration**
X	0	REF_{IN}/REF_{OUT}	External Reference (disable internal reference)
0	1	4.096V	Internal Reference
1	1	2.5V	Internal Reference

2.6 Linearization Function

Many bridge sensors have an inherently nonlinear output with applied pressure. Figure 2-9 illustrates a typical nonlinearity correction using the PGA309 linearization circuit.

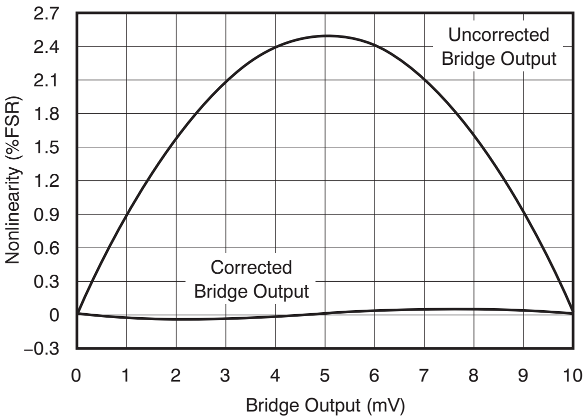
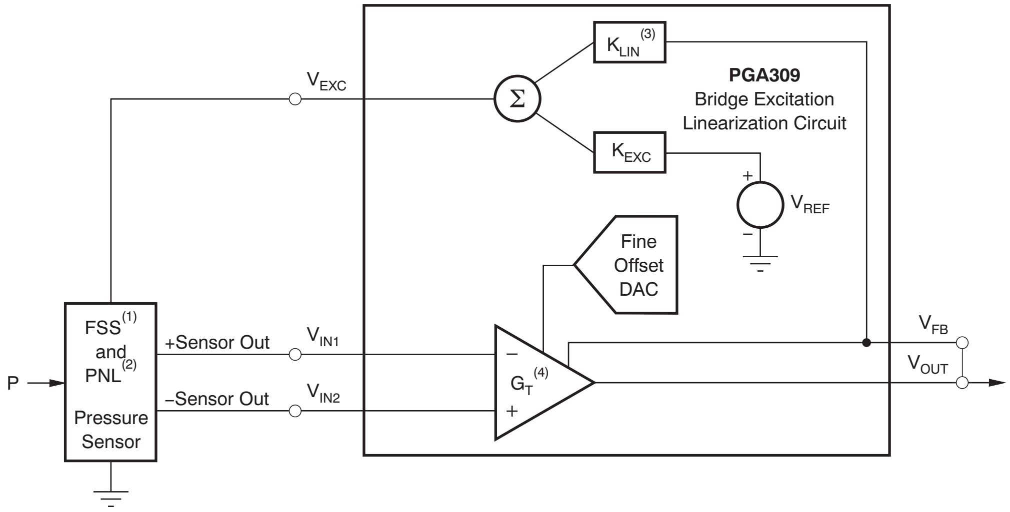


Figure 2-9. Bridge Pressure Nonlinearity Correction

The PGA309 contains a dedicated circuit for sensor voltage excitation and linearization, as shown in Figure 2-10. The Linearization Circuit scales the selected V_{REF} and sums it together with a portion of the output voltage (V_{OUT}) through the feedback pin (V_{FB}) to compensate for the bow-shaped nonlinearity of the bridge sensor output versus pressure. Using this technique, it is possible to compensate for parabolic nonlinearity resulting in up to to a 20:1 improvement over an uncompensated bridge output, as shown in Figure 2-9. K_{LIN} is a bipolar scale factor of V_{OUT} produced by the Lin DAC. K_{EXC} is a set attenuation factor of V_{REF} to allow for increases or decreases to V_{EXC}, as required. There are two ranges available in the Linearization Circuit, with a different respective range and a different respective fixed attenuation for K_{LIN}.



NOTE:

1. FSS = Full-Scale bridge Sensitivity of sensor.
2. PNL = Pressure Nonlinearity of sensor.
3. K_{LIN} = Linearization coefficient set by the Lin DAC.
4. G_T = (Front-End PGA Gain)(Gain DAC)(Output Amplifier Gain).

Figure 2-10. Bridge Excitation Linearization Circuit

If no sensor voltage excitation linearization is needed, there are several options for the bridge excitation. In ratiometric systems, the bridge should be tied directly to V_{SA}. In systems that provide an external reference for V_{REF}, the sensor should be tied to this external sensor. For systems that use the PGA309 internal reference, it is recommended that V_{EXC} be used for sensor excitation, and Lin DAC be set to zero. The reason for this is to minimize any large current draws from the REF_{IN}/REF_{OUT} pin that could affect the internal V_{REF} value used by the internal circuits.

In systems that do not use V_{EXC}, both the Lin DAC and V_{EXC} may be disabled by setting the appropriate Register 3 bits (10, 7:0) to ‘0’. This results in 50μA to 100μA of lower total quiescent current.

The typical bandwidth of the Linearization Circuit from the V_{FB} pin to V_{EXC} is 35kHz.

The output signal-dependence (V_{OUT} dependence) of the bridge excitation (V_{EXC}) adds a second-order term to the overall system transfer function (PGA309 + bridge sensor). The Lin DAC shown in Figure 2-11 scales a portion of V_{OUT} that is then summed with a scaled version of the reference voltage, V_{REF}. The Lin DAC code can be set to compensate for each individual bridge sensor nonlinearity. As illustrated in Figure 2-11, there are two ranges available in the PGA309 Linearization Circuit to accommodate a variety of sensor nonlinearities and V_{REF} combinations.

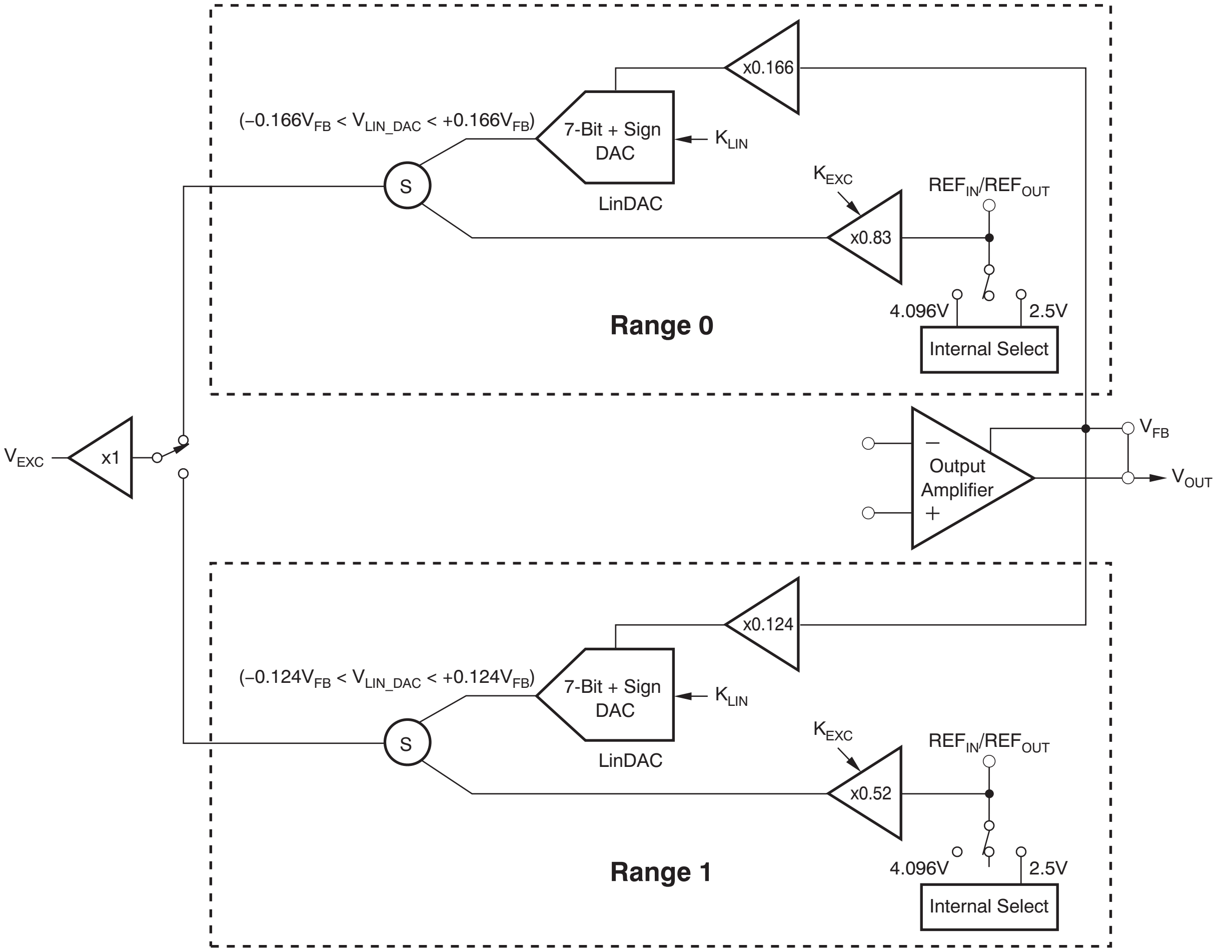


Figure 2-11. Linearization Circuit

To determine the value for the Lin DAC, also called the linearization coefficient K_{LIN}, the nonlinearity of the bridge sensor with constant excitation voltage must be known. The PGA309 linearization circuitry can only compensate for the parabolic-shaped portions of a sensor’s nonlinearity with applied pressure. This nonlinearity is assumed to be constant over temperature or the temperature variations are assumed to be an insignificant contribution to the system error budget. For the typical PGA309 application, the K_{LIN} factor is not adjusted with temperature changes. Optimum correction occurs when maximum deviation from a linear output occurs at mid-scale, as shown in Figure 2-12 and Figure 2-13. Sensors with nonlinearity curves similar to that of Figure 2-12, but not peaking at exactly mid-scale, can still be substantially improved. A sensor with an S-shaped nonlinearity curve (equal positive and negative nonlinearity) cannot be improved by using the PGA309 Linearization Circuit.

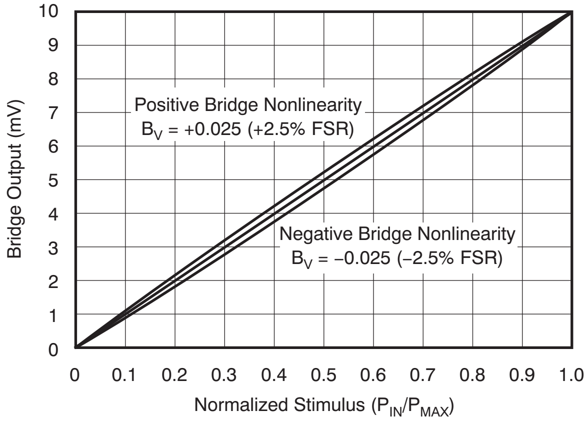


Figure 2-12. Bridge Output vs Pressure

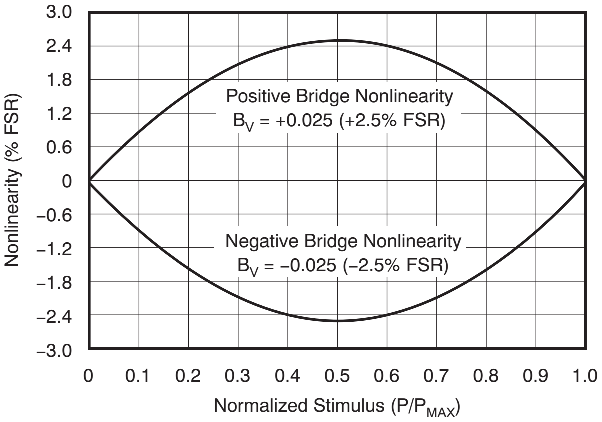


Figure 2-13. Bridge Nonlinearity (%FSR) vs Pressure

Either positive or negative bridge nonlinearities can be compensated by the proper setting of the Lin DAC polarity. To correct for positive bridge nonlinearity (upward bowing—shown in Figure 2-13), the Lin DAC value should be set positive. For negative bridge nonlinearity (downward bowing—shown in Figure 2-13), set the Lin DAC value negative.

The excitation voltage (V_{EXC}) directly scales the bridge sensor output, and therefore, must be accounted for in the gain and offset setting of the PGA309 when the linearization circuit is used.

Key definitions and design equations for the linearization circuit are given in the following sections.

2.6.1 System Definitions

B_V: Bridge Nonlinearity with Applied Pressure. Maximum error at mid-scale input range given as a decimal equivalent of % of full-scale range (%FSR). For Example, %FS: +2.5% FS = 0.025, −2.5% = −0.025.

FSS: Full-Scale Bridge Sensitivity for Sensor at PMAX (i.e., 5mV/V)

G_L: Total PGA309 Gain of V_{OUT}/V_{IN} when using the Linearization Circuit.

G_T: Total PGA309 Gain of V_{OUT}/V_{IN}.
G_T = (Front-End PGA Gain)(Gain DAC)(Output Amplifier Gain).

K_{EXC}: PGA Excitation Coefficient. Scale factor on V_{REF}.

K_{LIN}: PGA309 Linearization Coefficient

K_P: Pressure Constant. Converts linear input pressure to nonlinear pressure detected by sensor. Referenced to full-scale input pressure.

P: Pressure Input to Sensor

P_{MIN}: Minimum Sensor Input Pressure

P_{MAX}: Maximum Sensor Input Pressure

PNL: Nonlinear Pressure Output of Bridge with Linear Pressure Input P

V_{EXC}: Bridge Voltage Excitation (generated by PGA309 based on V_{REF}, K_{LIN}, K_{EXC}, V_{OUT})

$V_{OUT\ MIN}$: Minimum PGA309 V_{OUT} Voltage for P_{MIN} Bridge Sensor Input

$V_{OUT\ MAX}$: Maximum PGA309 V_{OUT} Voltage for P_{MAX} Bridge Sensor Input

V_{REF}: PGA309 Reference Voltage

2.6.2 Key Linearization Design Equations

The focus of this section is to define the design equations used to scale the PGA309 when using the Linearization Circuit.

Nonlinear Pressure Conversion for Bridge Sensor Parabolic Nonlinearity

$$PNL = P + 4(B_V) \bullet P_{MAX} \bullet \left[\left(\frac{P}{P_{MAX}}\right) - \left(\frac{P}{P_{MAX}}\right)^2\right]$$

B_V = positive for a positive parabolic nonlinearity, B_V = negative for a negative parabolic nonlinearity; see Figure 2-13) (2)

Pressure Constant (PNL referenced to full-scale input pressure)

$$K_P = \frac{PNL}{P_{MAX}}$$

$$K_P = \frac{\left(P + 4(B_V) \bullet P_{MAX} \bullet \left[\left(\frac{P}{P_{MAX}}\right) - \left(\frac{P}{P_{MAX}}\right)^2\right]\right)}{P_{MAX}} \quad (3)$$

Linearization Coefficient

$$K_{LIN} = \frac{4 \bullet B_V \bullet V_{REF} \bullet K_{EXC}}{(V_{OUT\_MAX} - V_{OUT\_MIN}) - 2 \bullet B_V \bullet (V_{OUT\_MAX} + V_{OUT\_MIN})} \quad (4)$$

Total PGA309 Gain Required When Using Linearization Circuit

$$G_L = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{REF} \bullet K_{EXC} \bullet FSS) + (K_{LIN} \bullet V_{OUT\_MAX} \bullet FSS)} \quad (5)$$

PGA309 V_{OUT}

$$V_{OUT} = \frac{(FSS \cdot G_L \cdot K_P \cdot V_{REF} \cdot K_{EXC}) + V_{OUT\_MIN}}{1 - (FSS \cdot G_L \cdot K_P \cdot K_{LIN})} \tag{6}$$

PGA309 V_{EXC}

$$V_{EXC} = V_{REF} \cdot K_{EXC} + K_{LIN} \cdot V_{OUT} \tag{7}$$

Lin DAC Counts Conversion

$$\text{Decimal \# Counts} = \frac{|K_{LIN}|}{(\text{Full-Scale Ratio} / 127)}$$

where Full-Scale Ratio = 0.166 (Range 0) or 0.124 (Range 1) (8)

Example 2-2. Lin DAC Counts Conversion

Given:

Range 0: $-0.166V_{FB}$ < Lin DAC < $+0.166V_{FB}$

Find:

Lin DAC value for $K_{LIN} = -0.082$

Solution:

1. Absolute value of $K_{LIN} = |-0.082| = 0.082$
2. Decimal # Counts = 0.082 / (0.166/127) = 62.7349
3. Use 63 counts → 3Fh → 0011 1111
4. However, −0.082 is needed. Add 1 in the sign bit (MSB, Bit 7) for negative ratio
5. Final Lin DAC setting: 1011 1111 → BFh

2.6.3 Key Ideal Design Equations

Ideal Gain, G

$$G_{IDEAL} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{REF} \cdot FSS} \tag{9}$$

V_{OUT} Ideal as a Function of Pressure, P

$$V_{OUT\_IDEAL} = FSS \cdot G_{IDEAL} \cdot \left(\frac{P}{P_{MAX}}\right) \cdot V_{REF} + V_{OUT\_MIN} \tag{10}$$

Full-Scale Range of Output

$$FSR = V_{OUT\_MAX} - V_{OUT\_MIN} \tag{11}$$

V_{OUT} Error (%FSR)

$$V_{OUT\_ERR\_FSR} = \left(\frac{V_{OUT} - V_{OUT\_IDEAL}}{FSR}\right) \cdot 100 \tag{12}$$

Example 2-3. Linearization Design

System Inputs	Value	Units
P_{MIN}	0	psi
P_{MAX}	100	psi
FSS	0.005	V/V
B_V	+0.025 (+0.025 = +2.5%)	%FSR
$V_{OUT\ MAX}$	4.5	V
$V_{OUT\ MIN}$	0.5	V
V_{REF}	5	V
K_{EXC}	0.83	
PGA309 Calculations for Using Linearization Circuit		
K_{LIN}	+0.110667	V/V
G_L	172.117	V/V
$V_{OUT\ IDEAL}$		
G_{IDEAL}	160	V/V
FSR	4	V

P (psi)	K_P	V_{OUT} (V)	V_{EXC} (V)	$V_{OUT\ IDEAL}$ (V)	V_{OUT} Error (%FSR)
0	0.0000	0.5000	4.2053	0.5000	0
10	0.1090	0.8986	4.2494	0.9000	−0.03464537
20	0.2160	1.2981	4.2937	1.3000	−0.04667445
30	0.3210	1.6983	4.3380	1.7000	−0.04126142
40	0.4240	2.0990	4.3823	2.1000	−0.02381898
50	0.5250	2.5000	4.4267	2.5000	1.1102E−14
60	0.6240	2.9010	4.4710	2.9000	0.02430134
70	0.7210	3.3017	4.5154	3.3000	0.04294918
80	0.8160	3.7020	4.5597	3.7000	0.04956629
90	0.9090	4.1015	4.6039	4.1000	0.03753519
100	1.0000	4.5000	4.6480	4.5000	2.2204E−14

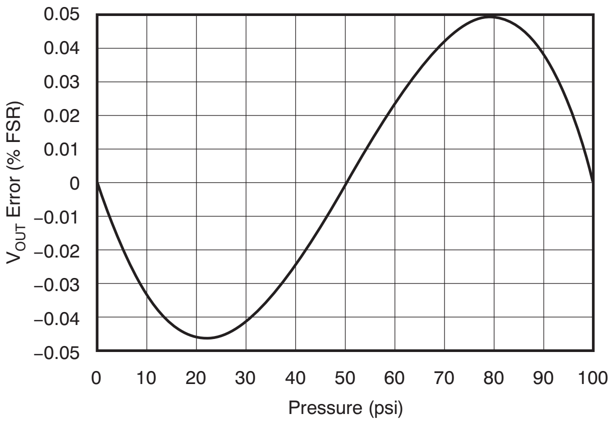


Figure 2-14. Corrected Bridge Parabolic Nonlinearity vs Pressure

In each end application, the Linearization Circuit limits should be checked for operation within the allowed range.

Table 2-5 and Table 2-6 illustrate the linearization range for several typical system applications. These tables account for the internal limits of the PGA309 linearization circuit and assume that V_{OUT} scaling is to account for over-scale and under-scale limits and fault detection. For specific end applications not listed, the following equations may be used to calculate critical design values, once the system design choices for V_{REF}, V_{OUTMAX},V_{OUTMIN} and linearization range, are made:

1. $V_{EXC\ MAX}$: Use Equation 7 at $V_{OUT\ MAX}$
2. $V_{EXC\ MIN}$: Use Equation 7 at $V_{OUT\ MIN}$
3. B_{VMAX} (maximum nonlinearity that can be compensated): Use $K_{LIN+MAX}$ to calculate $+B_{VMAX}$ and $K_{LIN–MAX}$ to calculate $–B_{VMAX}$ by Equation 4 solved for B_V as:

$$B_V = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{\left(\frac{4 \bullet V_{REF} \bullet K_{EXC}}{K_{LIN}}\right) + 4 \bullet (V_{OUT\_MAX} + V_{OUT\_MIN})}$$

   - For Range 0:
     $K_{LIN\ -MAX} = -0.166$
     $K_{LIN\ +MAX} = +0.166$
   - For Range 1:
     $K_{LIN\ -MAX} = -0.124$
     $K_{LIN\ +MAX} = +0.124$
4. $V_{Lin\ DAC\ MAX} = ((V_{REF}/4) – V_{OUT\ MAX}/10) \geq 300mV$
5. $V_{EXC\ MAX} \leq V_{SA} - 0.5V$
6. $K_{LIN\ -MAX} \leq K_{LIN} \leq K_{LIN\ +MAX}$

When using the Linearization Circuit, to ensure that the bridge sensor output common-mode voltage remains within the PGA309 input specifications, Equation 7 can be used to calculate V_{EXC} at full-scale signal ($V_{OUT\ MAX}$). The common-mode voltage (V_{CM}) of the bridge sensor output is one-half of V_{EXC} if no common-mode or temperature sensing additional resistor is used in series with the bridge sensor.

During the sensor calibration process using the PGA309, a two-step process can be employed. First, the nonlinearity of the sensor bridge is measured with an initial gain and offset and with $K_{LIN} = 0$ (Lin DAC set to Zero). Using the resulting sensor nonlinearity (B_V), values for K_{LIN}, Gain, and Offset are calculated. A second calibration measurement can be taken to adjust K_{LIN}, to account for any offsets and mismatches in the Linearization Circuit. This calibration procedure is most easily performed using the PGA309 Designer’s Kit and associated software and calibration spreadsheets, which can be downloaded from www.ti.com.

Table 2-4. PGA309 Recommended Operating Conditions

Case1	Case2	Case3	Case4	
0.057	0.075	0.112	0.075	$K_{LIN\ +MAX}$

Range 0					
K_{EXC}	0.83		FSS	0.005	V/V
$K_{LIN\ +MAX}$	–0.166				
$K_{LIN\ –MAX}$	0.166				

Table 2-5. Range 0—Typical System Applications and Maximum Nonlinearity Correction

						RANGE 0 $+B_{V\ MAX}$				RANGE 0 $-B_{V\ MAX}$				RANGE 0
$V_{SA\ MIN}$ (V)	$V_{SA\ MAX}$ (V)	V_{REF} (V)	ADC REF (V)	$V_{OUT\ MIN}$ (V)	$V_{OUT\ MAX}$ (V)	$+B_V$ (0.025= 2.5%)	$V_{EXC\ MAX}$ (1) (V)	$V_{EXC\ MIN}$ (V)	G	$-B_V$ (−0.025= −2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G	LinDAC MAX > 0.3V? (V)
2.7	5.5	2.5	2.5	0.175	2.225	0.0136	2.202	2.104	167.73	−0.0454	2.046	1.706	240.38	0.4025
2.7	5.5	2.5	2.048	0.123	1.761	0.0143	2.207	2.095	138.38	−0.0354	2.055	1.783	183.77	0.4489
4.5	5.5	4.096	2.5	0.175	2.175	0.0231	3.761	3.429	106.36	−0.0259	3.371	3.039	131.64	0.8065
4.5	5.5	4.096	4.096	0.246	3.564	0.0371	3.991	3.441	166.26	−0.0447	3.359	2.808	236.32	0.6676
4.5	5.5	4.096	2.048	0.143	1.782	0.0191	3.695	3.423	88.70	−0.0210	3.376	3.104	105.61	0.8458
4.7	5.5	4.5	4.5	0.27	4.185	0.0275	4.204	3.780	176.76	−0.0483	3.690	3.040	257.54	0.7065
5	5.5	5	5	0.3	4.65	0.0188	4.499	4.200	176.76	−0.0483	4.100	3.378	257.54	0.785

(1) Limited by V_{EXC} saturation voltage of 0.5V.

Table 2-6. Range 1—Typical System Applications and Maximum Nonlinearity Correction(1)(2)(3)

PGA309 V_{SA} Operating Range		PGA309 V_{REF}	System ADC REF	PGA309 V_{OUT} Linear Range		PGA309 $+B_{V\ MAX}$	PGA309 V_{EXC} Range for $+B_{V\ MAX}$		PGA309 Gain $V_{OUT}/V_{DIFF\ IN}$ for $+B_{V\ MAX}$	PGA309 $-B_{V\ MAX}$	PGA309 V_{EXC} Range for $-B_{V\ MAX}$		PGA309 Gain $V_{OUT}/V_{DIFF\ IN}$ for $-B_{V\ MAX}$	PGA309 LinDAC Max Check
						RANGE 0 $+B_{V\ MAX}$				RANGE 0 $-B_{V\ MAX}$				RANGE 0
$V_{SA\ MIN}$ (V)	$V_{SA\ MAX}$ (V)	V_{REF} (V)	ADC REF (V)	$V_{OUT\ MIN}$ (V)	$V_{OUT\ MAX}$ (V)	$+B_V$ (0.025= 2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G_T	$-B_V$ (−0.025= −2.5%)	$V_{EXC\ MAX}$ (V)	$V_{EXC\ MIN}$ (V)	G_T	LinDAC MAX > 0.3V? (V)
2.7	5.5	2.5	2.5	0.175	2.225	0.0439	1.576	1.322	260.17	−0.0552	1.278	1.024	400.35	0.4025
2.7	5.5	2.5	2.048	0.123	1.761	0.0358	1.518	1.315	215.76	−0.0429	1.285	1.082	302.87	0.4489
4.5	5.5	4.096	2.5	0.175	2.175	0.0272	2.400	2.152	166.69	−0.0312	2.108	1.860	215.03	0.8065
4.5	5.5	4.096	4.096	0.246	3.564	0.0435	2.572	2.160	258.02	−0.0543	2.099	1.688	393.13	0.6676
4.5	5.5	4.096	2.048	0.143	1.782	0.0226	2.351	2.148	139.44	−0.0253	2.112	1.909	171.72	0.8458
4.7	5.5	4.5	4.5	0.27	4.185	0.0464	2.859	2.373	273.88	−0.0588	2.307	1.821	429.97	0.7065
5	5.5	5	5	0.3	4.65	0.0464	3.177	2.637	273.88	−0.0588	2.563	2.023	429.97	0.785

(1) Over-scale and under-scale limits and fault detection desired.

(2) FSS used to calculate a representative gain value (G_T) for completeness.

(3) Range 1, $K_{EXC} = 0.52$, $K_{LIN\ -MAX} = -0.124$, $K_{LIN\ +MAX} = 0.124$, FSS = 0.005V/V

2.7 Temperature Measurement

The center of the PGA309 temperature measurement circuitry is the Temp ADC. The Temp ADC and its associated PGA, input mux, and REF mux provide a flexible and configurable temperature sensing block for reading either on-chip or external temperatures. Figure 2-15 illustrates the PGA309 temperature sense block.

The internal temperature sensing is accomplished by using on-chip diode junctions. The Internal Temperature Mode is configured through setting the bits in Register 6 to the values shown in Table 2-7 and Table 2-8. The Temp ADC output is presented in Register 0 in 12-bit + sign extended, right-justified, two's complement data format (see Table 2-9). The resolution, for the Temp ADC in Internal Temperature Mode, is 0.0625°C/count and the accuracy is ±2°C. The temperature accuracy is a relative error that is calibrated out with the PGA309 + sensor calibration to the accuracy of the calibration temperature measurement equipment.

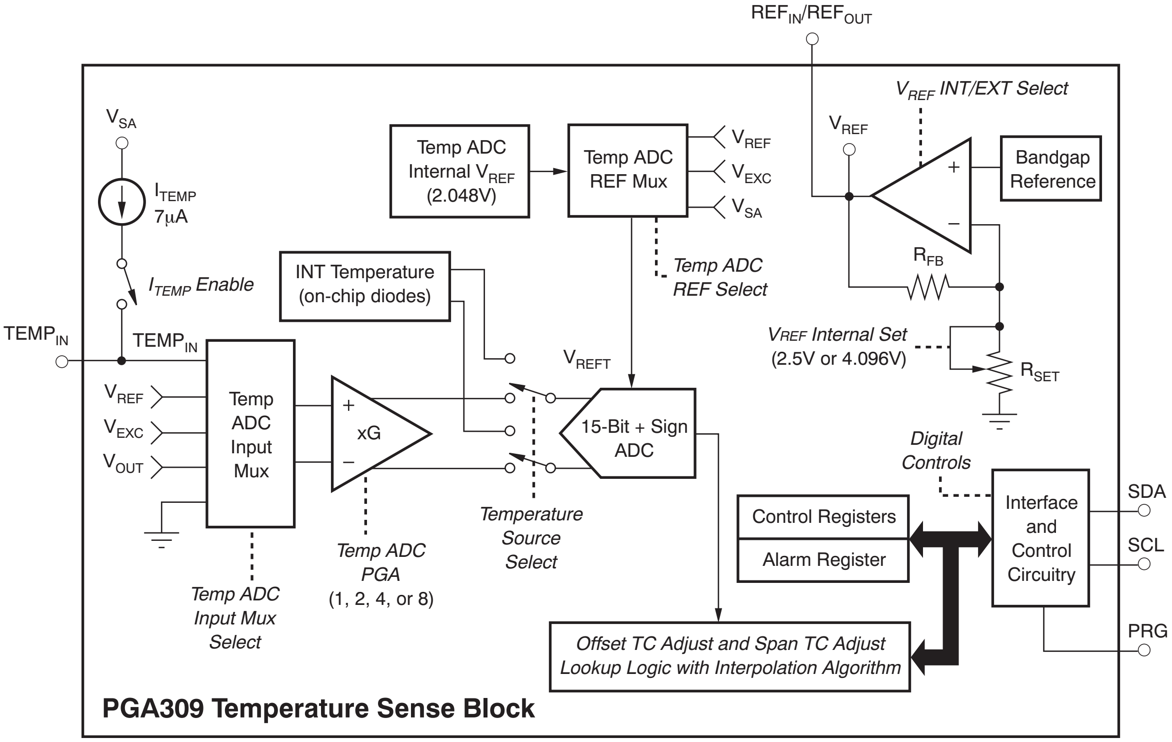


Figure 2-15. Temperature Sense Block

Table 2-7. Internal Temperature Mode Configuration—Register 6

Bit	Bit Name	Bit State	Configuration
15	RFB	0	Reserved Factory Bit—set to 0 for proper operation
14	RFB	0	Reserved Factory Bit—set to 0 for proper operation
13	ADC2X	0	Unused for Internal Temperature Mode; set to zero.
12	ADCS	0	
11	ISEN	0	
10	CEN	1	Enable the Temp ADC
9	TEN	1	Internal Temperature Mode selected
8	AREN	0	Unused for Internal Temperature Mode; set to zero.
7	RV1	0	
6	RV0	0	
5	M1	0	
4	M0	0	
3	G1	0	
2	G0	0	
1	R1	1	See Table 2-8.
0	R0	1	See Table 2-8.

Table 2-8. Internal Temperature Mode Resolution—Register 6

R1	R0	Temp ADC Resolution (Conversion Time) Select TEN = ‘1’
0	0	9-Bit + Sign, Right-Justified, Sign-Extended, Twos Complement, 0.5°C (3ms)
0	1	10-Bit + Sign, Right-Justified, Twos Complement, Sign-Extended, 0.25°C (6ms)
1	0	11-Bit + Sign, Right-Justified, Twos Complement, Sign-Extended, 0.125°C (12ms)
1	1	12-Bit + Sign, Right-Justified, Twos Complement, Sign-Extended, 0.0625°C (24ms)

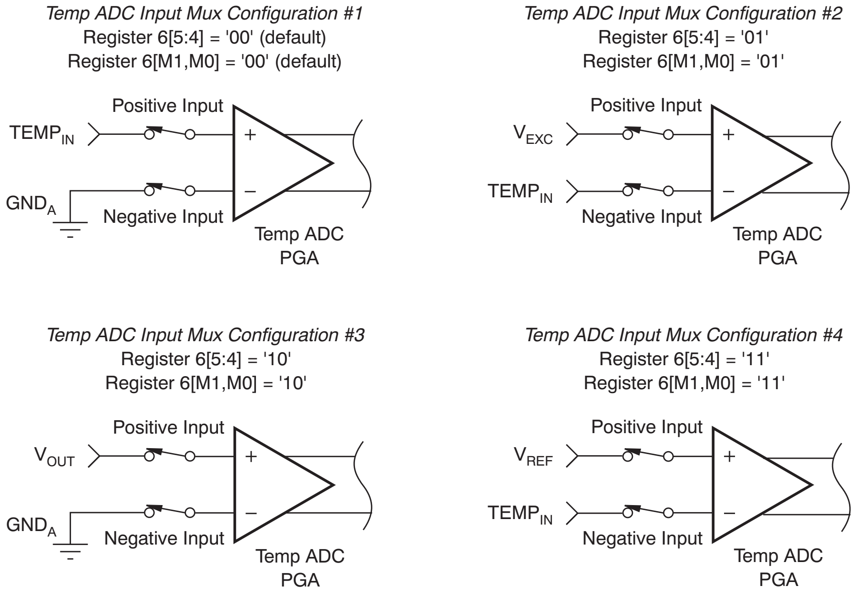
Table 2-9. Internal Temperature Mode Data —Register 0(1)

Temperature (°C)	Digital Output (Binary) AD15…………AD0	Digital Output (Hex)
128	0000 1000 0000 0000	0800
127.9375	0000 0111 1111 1111	07FF
100	0000 0110 0100 0000	0640
80	0000 0101 0000 0000	0500
75	0000 0100 1011 0000	04B0
50	0000 0011 0010 0000	0320
25	0000 0001 1001 0000	0190
0.25	0000 0000 0000 0100	0004
0.0	0000 0000 0000 0000	0000
−0.25	1111 1111 1111 1100	FFFC
−25	1111 1110 0111 0000	FE70
−55	1111 1100 1001 0000	FC90
−128	1111 1000 0000 0000	F800

(1) The resolution for the Temp ADC in Internal Temperature Mode is 0.0625°C/count.
For Positive Temperatures (for example, +50°C):
Twos Complement is not performed on positive numbers. Therefore, simply convert the number to binary code with the 16-bit, right-justified format, and MSB = 0 to denote a positive sign. Extend this sign into the upper 4 bits.
Example: (50°C)/(0.0625°C/count) = 800 = 320h = 0011 0010 0000 Twos Complement 16-bit, right-justified, sign-extended format = 0000 0011 0010 0000 = 0320h.
For Negative Temperatures (for example, −25°C):
Generate the Twos Complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number with MSB = 1. Extend the sign to the upper 4 bits to form the 16-bit word.
Example: (| −25°C|)/(0.0625°C/count) = 400 = 190h = 0001 1001 0000 Twos Complement format: 1110 0111 0000 Extend the sign and create the 16-bit word: 1111 1110 0111 0000 = FE70h

There are several configurations possible for the Temp ADC when External Temperature Mode is selected. In this mode, the $TEMP_{IN}$ pin is read to determine temperature. $TEMP_{IN}$ may be referenced to GND, V_{EXC}, or V_{REF}. V_{OUT} may also be selected to be read relative to GND through the Temp ADC. Figure 2-16 shows the allowable Temp ADC input mux configurations.

NOTE: In Configuration #3, the V_{OUT} pin is read, not the V_{FB} pin. Therefore, this value may be different from $V_{OUT\ FILT}$. Refer to Figure 1-1 and Figure 2-5.



Temp ADC Input Mux Configuration #1
Register 6[5:4] = '00' (default)
Register 6[M1,M0] = '00' (default)

Temp ADC Input Mux Configuration #2
Register 6[5:4] = '01'
Register 6[M1,M0] = '01'

Temp ADC Input Mux Configuration #3
Register 6[5:4] = '10'
Register 6[M1,M0] = '10'

Temp ADC Input Mux Configuration #4
Register 6[5:4] = '11'
Register 6[M1,M0] = '11'

Figure 2-16. Temp ADC Input Mux Options

Table 2-10. Temp ADC PGA Gain Select—Register 6

G1 [3]	G0 [2]	Temp ADC PGA Gain
0	0	1
0	1	2
1	0	4
1	1	8

The temperature sense block also contains a 7µA (typ) current source, I_{TEMP}, that is enabled by a logic ‘1’ written to Register 6, bit 11, ISEN. A logic ‘0’ disables I_{TEMP} from the $TEMP_{IN}$ pin. This current source can be used to excite an external resistive temperature device or diode for bridge sensor temperature measurement, as shown in Figure 2-17.

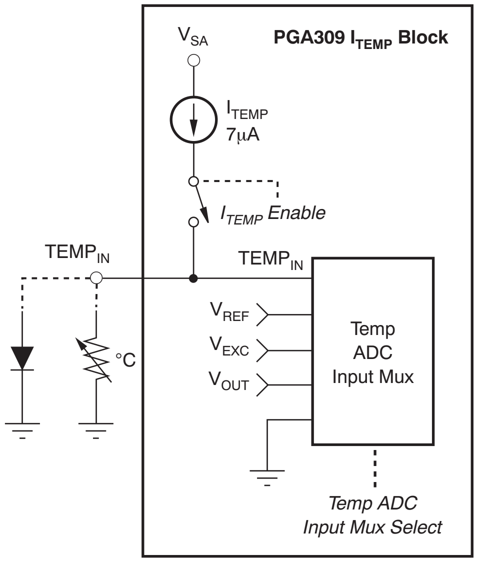


Figure 2-17. I_{TEMP} for External Temperature Measurement

The Temp ADC has several choices for its reference voltage for analog-to-digital conversions when used in External Temperature mode; these are illustrated in Table 2-11 and Figure 2-15. The resolution of the Temp ADC when used in External Temperature mode is also register-selectable (see Table 2-12).

Table 2-11. Temp ADC Reference Select—Register 6

AREN [8]	RV1 [7]	RV0 [6]	Temp ADC Reference (V_{REFT})
0	0	0	V_{REF}
0	0	1	V_{EXC}
0	1	0	V_{SA}
0	1	1	Factory Reserved
1	X[1]	X[1]	Temp ADC Internal REF (2.048V)

[1] ‘X’ = don’t care.

Table 2-12. Temp ADC[1] Resolution (Conversion time)—Register 6

R1 [1]	R0 [0]	External Signal Mode [TEN=0], External Reference [AREN=0]	External Signal Mode [TEN=0], Internal Reference [2.048V, AREN=1]
0	0	11-Bit + Sign, Right-Justified, Sign-Extended (6ms)	11-Bit + Sign, Right-Justified, Sign-Extended (8ms)
0	1	13-Bit + Sign, Right-Justified, Sign-Extended (24ms)	13-Bit + Sign, Right-Justified, Sign-Extended (32ms)
1	0	14-Bit + Sign, Right-Justified, Sign-Extended (50ms)	14-Bit + Sign, Right-Justified, Sign-Extended (64ms)
1	1	15-Bit + Sign, Right-Justified, Sign-Extended (100ms)	15-Bit + Sign, Right-Justified, Sign-Extended (128ms)

[1] Temp ADC uses Twos Complement data format.

2.7.1 *Temp ADC Start-Convert Control*

The Temp ADC has two conversion modes: Single and Continuous. In Continuous Conversion mode (CEN = ‘1’), the Temp ADC initiates the next conversion cycle immediately after a conversion is complete. In Single Conversion mode (CEN = ‘0’) the Temp ADC start-convert bit (ADCS) acts as a start-convert/busy bit and must be set to ‘1’ before a conversion is initiated. Setting ADCS to ‘1’ occurs when the register configuration section of the EEPROM (part one) contains ADCS = ‘1’ and the EEPROM is read. Furthermore, ADCS will be reset to ‘1’ for each successive EEPROM read. After ADCS is set to ‘1’, it will be a ‘1’ if read immediately and can be polled until it returns to a ‘0’, indicating the conversion is complete. The Start-Convert modes are shown in Table 2-13.

Table 2-13. Temp ADC Start-Convert Control—Register 6

CEN [10]	ADCS [12]	Conversion Mode	Comments
0	0	Single	Temp ADC mode—no conversions.
0	1	Single	Temp ADC starts conversion and ADCS acts as busy bit with it changing to a '0' at end of conversion.
1	X	Continuous	ADCS bit excercises no control—typically ADCS = '1' since conversions are continuous

In Figure 2-18 continuous start-convert control is selected. After an initial power-on reset timeout of typically 33ms, the register configuration section of the EEPROM (part one) is read. Immediately after this, a Temp ADC conversion is started. At the end of this first conversion, the temperature coefficients section of the EEPROM (part two) are read, and Zero and Gain DAC settings are adjusted. Since CEN = ‘1’, the end of each conversion will start the next conversion. After the temperature coefficients section of the EEPROM (part two) has been read, the register configuration values are read. Note that reading of the second half of the EEPROM (temperature coefficients) is triggered by a valid register configuration read of the EEPROM. This operation yields the most temperature updates over a given time period.

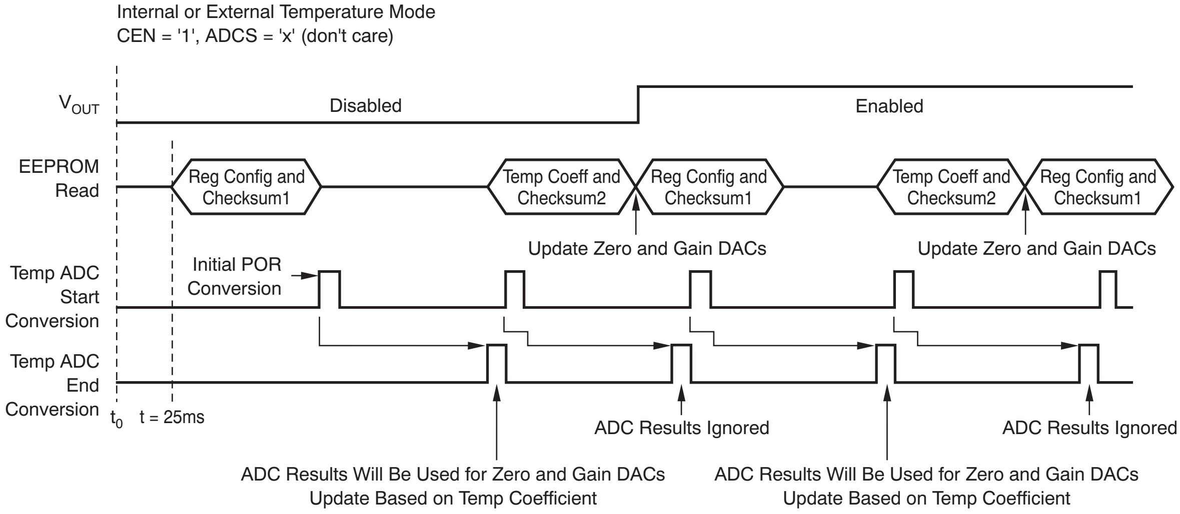


Figure 2-18. Temp ADC Continuous Start-Convert Control

In Figure 2-19, Single Conversion mode is selected (CEN = ‘0’). After an initial power-on reset timeout of typically 33ms, the register configuration (part one) of the EEPROM is read. Immediately after this, a Temp ADC conversion is started if CEN = ‘0’ and ADCS = ‘1’. At the end of this first conversion, the temperature coefficients (part two) of the EEPROM are read, and Zero and Gain DAC settings are adjusted. When CEN = ‘0’ and ADCS = ‘1’, a new start conversion occurs only after reading the register configuration part of the EEPROM. At the end of this conversion, the second part of the EEPROM (temperature coefficients) is read, the Gain and Zero DAC temperature calculations are done, and each respective DAC updated. Note that in the Single Start-Convert mode, if CEN = ‘0’ and ADCS = ‘0’ (no Temp ADC conversions), the PGA309 will wait 33ms after power-on, read the register configuration part of the EEPROM, and without an ADC conversion, read the Lookup Table and calculate Gain and Zero DAC values. These values are based on the current ADC output register (all zero on power-up). The PGA309 output will then be enabled and will wait about 25ms, and read the register configuration part of the EEPROM. The output remains enabled with a continuous loop of reading the register configuration part of the EEPROM, waiting 33ms, and read again.

One final control option for External Temperature Mode is the ADC2X bit, Register 6 bit [13]. This bit allows the conversion speed of the Temp ADC to be increased for external temperature readings only.

Table 2-14 shows the typical settings and the effect of the ADC2X bit.

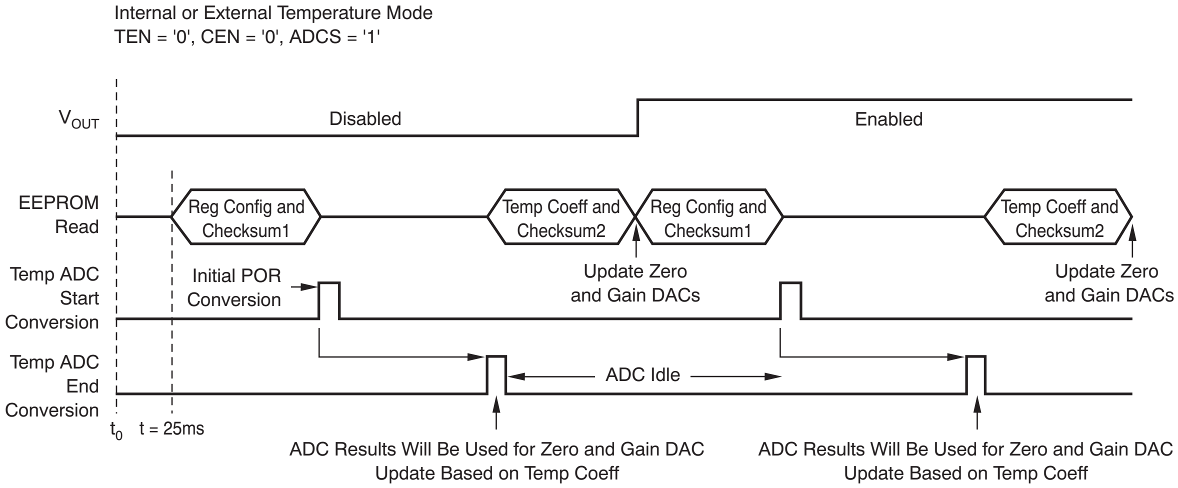


Figure 2-19. Temp ADC Single Start-Convert Control

Table 2-14. Temp ADC[1] Conversion Speed Options for External Temperature Mode

R1 [1]	R0 [0]	TEN=0], [AREN=0], [ADC2X=0]	[TEN=0], [AREN=0], [ADC2X=1]	[TEN=0] [2.048V, AREN=1], [ADC2X=0]	[TEN=0] [2.048V, AREN=1], [ADC2X=1]
0	0	11-Bit + Sign (6ms)	11-Bit + Sign (3ms)	11-Bit + Sign (8ms)	11 Bit + Sign (4ms)
0	1	13-Bit + Sign (24ms)	13-Bit + Sign (12ms)	13-Bit + Sign (32ms)	13 Bit + Sign (16ms)
1	0	14-Bit + Sign (50ms)	14-Bit + Sign (25ms)	14-Bit + Sign (64ms)	14 Bit + Sign (32ms)
1	1	15-Bit + Sign (100ms)	15-Bit + Sign (50ms)	15-Bit + Sign (128ms)	15 Bit + Sign (64ms)

(1) Temp ADC data uses a 16-bit, sign-extended, right-justified Twos Complement data format.

2.7.2 External Temperature Sensing with an Excitation Series Resistor

Some bridge sensor applications measure the temperature of the bridge sensor by the change in the bridge resistance. This is accomplished by adding a series resistor in either the top or the bottom of the bridge excitation connections. When this is done, the common-mode voltage range of the PGA309 inputs must be observed over the operating temperature range of the application.

Figure 2-20 shows a top-side series resistor (R_{T+}) used to monitor the change in bridge resistance with temperature. For simplification of analysis, the effective bridge resistance is converted to one resistor (R_{BT}), as shown. For a given temperature, R_{BT} will be a fixed value; for this example, 1.8kΩ at 70°C. Since R_T has a negligible change in temperature (50ppm/°C) compared with R_{BT} (3500ppm/°C), R_T is used to detect a change in R_{BT}. For this application, the Temp PGA is configured for V_{EXC} on the +input, and $TEMP_{IN}$ on the –input. The Temp ADC uses V_{EXC} as its reference, V_{REFT}. The Temp PGA is set to a gain of 8. Notice that two different values for V_{EXC} will be analyzed to emulate the changing voltage on V_{EXC} due to the linearization block adjusting V_{EXC} to minimize error on the bridge sensor output with applied pressure. The squareboxed values show numerical results for V_{EXC} = 2.9V and the oval-ringed values for V_{EXC} = 2.4V. The final Temp ADC reading will be the same value regardless of what value V_{EXC} is used by the linearization block.

Figure 2-21 shows a bottom-side series resistor (R_{T-}) used to monitor the change in bridge resistance with temperature. Again, for simplification of analysis, the effective bridge resistance is converted to one resistor (R_{BT}) as shown. For 70°C, R_{BT} is 1.8kΩ for this example. R_T is used to measure the change in R_{BT}. The Temp PGA is configured for $TEMP_{IN}$ on the +input and GND on the –input. VE_{XC} is selected as the Temp ADC reference, V_{REFT}. The PGA gain is 8. The square-boxed values are results for V_{EXC} = 2.9V and the oval-ringed values for V_{EXC} = 2.4V. It is seen that the final Temp ADC reading will be the same regardless of the V_{EXC} value.

If the linearization block is not used in the application, the bridge sensor top excitation connection is made to either V_{SA} or V_{REF}, instead of V_{EXC}. In either of these cases, top-side (Figure 2-20) or bottom-side (Figure 2-21), external temperature sensing can be done by adding a series resistor, R_T. The Temp ADC reference (V_{REFT}) should be changed to the bridge excitation voltage (V_{SA} or V_{REF}) for the specific application. This yields a constant Temp ADC output at a given temperature independent of changes in the bridge excitation voltage.

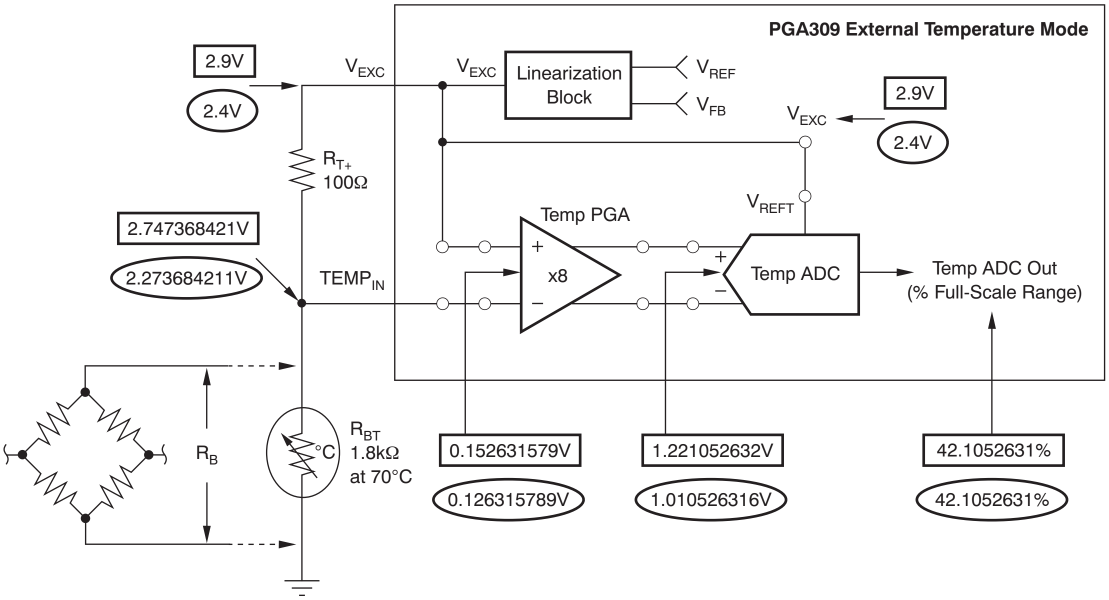


Figure 2-20. External Temperature Sensing of Bridge Sensor with Top-Side Series Resistor

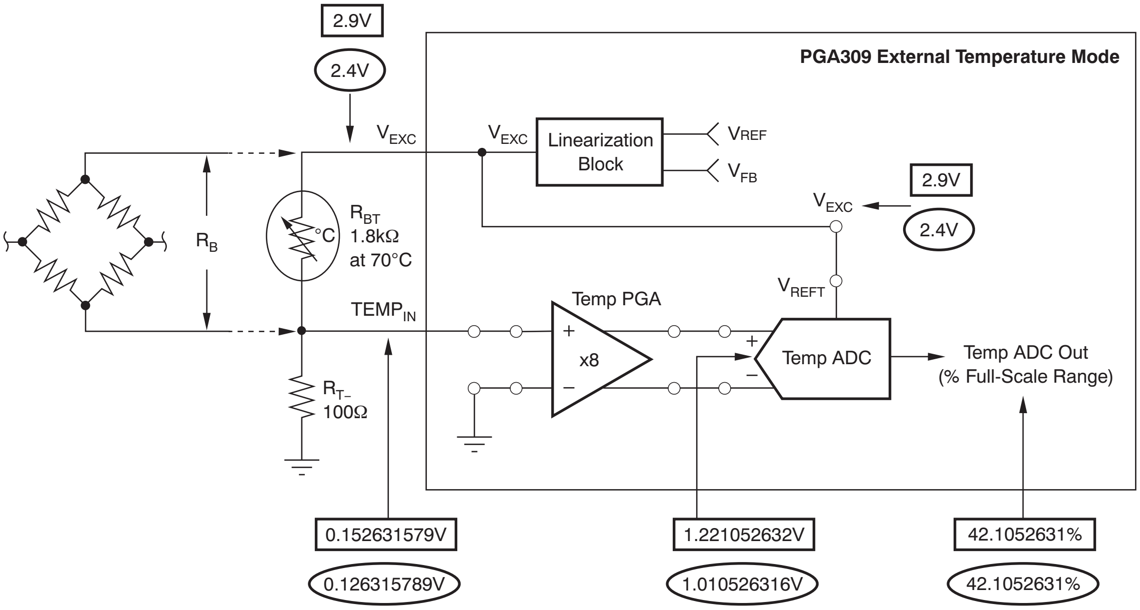
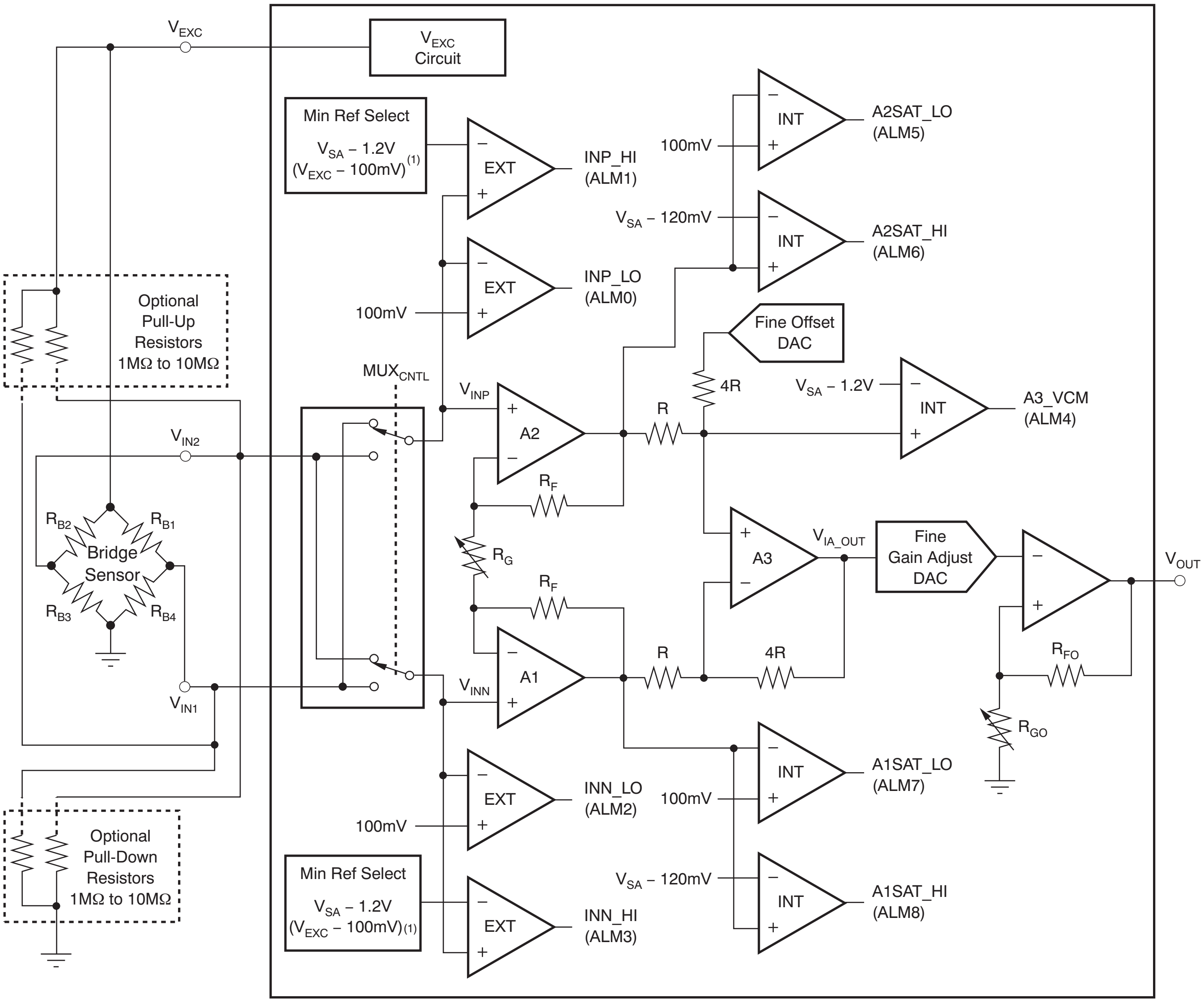


Figure 2-21. External Temperature Sensing of Bridge Sensor with Bottom-Side Series Resistor

2.8 Fault Monitor

Fault monitoring of external bridge sensors is provided on the PGA309 through nine internal comparators. Refer to Figure 2-22. These comparators are grouped into two sets: Internal Fault Comparators and External Fault Comparators. In Figure 2-22, these are denoted as EXT for those in the External Fault Comparator group and by INT for those in the Internal Fault Comparator group.



NOTE:

1. When V_{EXC} is enabled, a minimum reference selector circuit becomes the reference for the INN_HI and INP_HI comparator threshold. This minimum reference selector circuit uses V_{EXC} − 100mV and V_{SA} − 1.2V, and compares the V_{INX} pin to the lower of the two references. This ensures accurate fault monitoring in conditions where V_{EXC} might be higher or lower than the input voltage range of the Front-End PGA amplifier relative to V_{SA}.
2. All comparator outputs are high for fault condition.

Figure 2-22. PGA309 Fault Monitor Circuitry

The external fault comparators are used to monitor proper operation of the bridge sensor and report input fault conditions. Table 2-15 enumerates the possible fault cases for a bridge sensor and the associated fault comparator outputs for each fault condition. Due to the extremely low input bias currents of the PGA309, if fault detection of floating inputs (sensor disconnected entirely from one or both of the PGA309 inputs) is to be accurately reported, it is necessary to add either pull-up or pull-down resistors to each of these inputs (V_{IN1} and V_{IN2}), shown in Figure 2-22 as optional. The value of these resistors can be between 1MΩ and 10MΩ in order to minimize signal loading of the bridge sensor's output. Offset and other errors from these optional resistors will be cancelled out during the PGA309 + sensor calibration. Table 2-16 itemizes the special cases for floating inputs on the PGA309 when using pull-up resistors. Table 2-17 lists the special cases for floating inputs on the PGA309 when using pull-down resistors. All other fault cases not listed as special cases are the same as those detailed in Table 2-15.

Table 2-15. Bridge Sensor Faults and Fault Comparator States—V_{IN1} and V_{IN2} Have No Pull-Up or Pull-Down Resistors(1)

Case	V_{IN2} (V_{INN}) (V)	V_{IN1} (V_{INP}) (V)	VIA_OUT (V)	Logic Level Outputs				Comments
				INN_HI (ALM3)	INN_LO (ALM2)	INP_HI (ALM1)	INP_LO (ALM0)	
Normal	1.7	1.7	Linear	0	0	0	0	
R_{B1} Open	1.7	0	~0	0	0	0	1	
R_{B2} Open	0	1.7	~V_{SA}	0	1	0	0	
R_{B3} Open	3.4	1.7	~0	1	0	0	0	
R_{B4} Open	1.7	3.4	~V_{SA}	0	0	1	0	
R_{B1} Short	1.7	3.4	~V_{SA}	0	0	1	0	
R_{B2} Short	3.4	1.7	~0	1	0	0	0	
R_{B3} Short	0	1.7	?	0	1	0	0	
R_{B4} Short	1.7	0	~0	0	0	0	1	
Open Sensor GND	3.4	3.4	~0	1	0	1	0	
Open Sensor V_{EXC}	0	0	~0	0	1	0	1	
V_{EXC} Short GND	0	0	~0	1(2)	1	1(2)	1	
V_{IN1} (V_{INP}) Open(3)	1.7	~V_{SA}−0.7	~V_{SA}	0	0	0	0	Under-scale limit on V_{OUT}, no fault detect—Int or Ext
V_{IN2} (V_{INN}) Open(3)	~V_{SA}−0.7	1.7	~0	0	0	0	0	Over-scale limit on V_{OUT}, no fault detect—Int or Ext
V_{IN1} (V_{INP}) Short GND	1.7	0	~0	0	0	0	1	
V_{IN2} (V_{INN}) Short GND	0	1.7	~V_{SA}	0	1	0	0	
V_{IN1} (V_{INP}) Short V_{EXC}	1.7	3.4	~V_{SA}	0	0	1	0	
V_{IN2} (V_{INN}) Short V_{EXC}	3.4	1.7	~0	1	0	0	0	
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Open(3)	~V_{SA}−0.7	~V_{SA}−0.7	Linear?	0	0	0	0	Typically drifts to over-scale limit slowly; no Ext Fault detect (ALM7), Int Fault set = A1 Sat Low
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Short GND	0	0	~V_{SA}	0	1	0	1	
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Short V_{EXC}	3.4	3.4	~0	1	0	1	0	

(1) V_{SA} = +5V, V_{REF} = +4.096V, K_{EXC} = 0.83, K_{LIN} = 0, and V_{EXC} = 3.4V.

(2) Typically, a logic 1, but not ensured by design and nature of fault.

(3) Accurate detection of these faults requires a pull-up or pull-down resistor on each input (V_{IN1} and V_{IN2}).

Table 2-16. Bridge Sensor Faults and Fault Comparator States—V_{IN1} and V_{IN2} are connected by 10MΩ Pull-Up Resistors to V_{EXC} (1)

Special Case (2)	V_{IN2} (V_{INN}) (V)	V_{IN1} (V_{INP}) (V)	VIA_OUT (V)	Logic Level Outputs			
				INN_HI (ALM3)	INN_LO (ALM2)	INP_HI (ALM1)	INP_LO (ALM0)
V_{IN1} (V_{INP}) Open	1.7	V_{EXC}	~V_{SA}	0	0	1	0
V_{IN2} (V_{INN}) Open	V_{EXC}	1.7	~0	1	0	0	0
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Open	V_{EXC}	V_{EXC}	~0	1	0	1	0

(1) V_{SA} = +5V, V_{REF} = +4.096V, K_{EXC} = 0.83, K_{LIN} = 0, and V_{EXC} = 3.4V.

(2) All other cases not listed are the same as those in Table 2-15.

Table 2-17. 16.Bridge Sensor Faults and Fault Comparator States—V_{IN1} and V_{IN2} are connected by 10MΩ Pull-Down Resistors to GND(1)

Special Case (2)	V_{IN2} (V_{INN}) (V)	V_{IN1} (V_{INP}) (V)	VIA_OUT (V)	Logic Level Outputs			
				INN_HI (ALM3)	INN_LO (ALM2)	INP_HI (ALM1)	INP_LO (ALM0)
V_{IN1} (V_{INP}) Open	1.7	~0	~V_{SA}	0	0	0	1
V_{IN2} (V_{INN}) Open	~0	1.7	~0	0	1	0	0
V_{IN1} (V_{INP}), V_{IN2} (V_{INN}) Open	~0	~0	~0	0	1	0	1

(1) V_{SA} = +5V, V_{REF} = +4.096V, K_{EXC} = 0.83, K_{LIN} = 0, and V_{EXC} = 3.4V.

(2) All other cases not listed are the same as those in Table 2-15.

When V_{EXC} is enabled, external fault comparators INP_HI and INP_LO have a minimum reference selector circuit that selects between a typical trip point of either V_{EXC} – 100mV or V_{SA} – 1.2V. This ensures accurate fault monitoring in conditions where the Linearization Circuit increases V_{EXC}, and the bridge sensor has fault conditions that violate the IVR, relative to V_{SA}, of the Front-End PGA in the PGA309. If V_{EXC} is disabled, these comparators default to the V_{SA} – 1.2V threshold.

The internal fault comparators are used to monitor the Front-End PGA internal nodes of the PGA309 (see Figure 2-22). When PGA309 + Sensor calibration is in process, it is crucial to have the internal comparator group enabled because it can alert the user to an internal node violation. Such a violation may still yield an output voltage within the expected linear range, but it will not be an accurate one. Each of the front-end amplifiers, A1 and A2, of the Front-End PGA have their outputs monitored for both saturation to the positive supply or to ground. If either of these comparators trips during calibration, it is an indication of an out-of-range scaling condition due either to the incorrect Front-End PGA gain select or coarse offset adjust. The A3 amplifier in the Front-End PGA is also monitored for common-mode violations that can occur if the Zero DAC is combined incorrectly with the Front-End PGA gain select.

Each individual internal and external fault comparator can be read through one of the digital interfaces: Two-Wire or One-Wire. The current results are stored in Register 8—Alarm Status Register. When the PGA309 output is enabled, the value of the Alarm Status Register reflects the current state of the fault comparators. When V_{OUT} is disabled, the value in the register is the comparator status immediately before the output was disabled. This allows for easier identification and debugging of a three terminal sensor module (PRG shorted to V_{OUT}). See Section 4.10, *One-Wire Operation with PRG Connected to* V_{OUT}, for details. In addition, each group of comparators, internal fault and external fault, can be programmed such that if any comparator in their respective group is logic high, indicating a fault, the PGA309 output (V_{OUT}) will be forced to a fault indicating voltage level of either positive (V_{SA} − 0.1V max with a 10kΩ load) or negative (0.1V max with a 10kΩ load). The logic for this is shown in Figure 2-23.

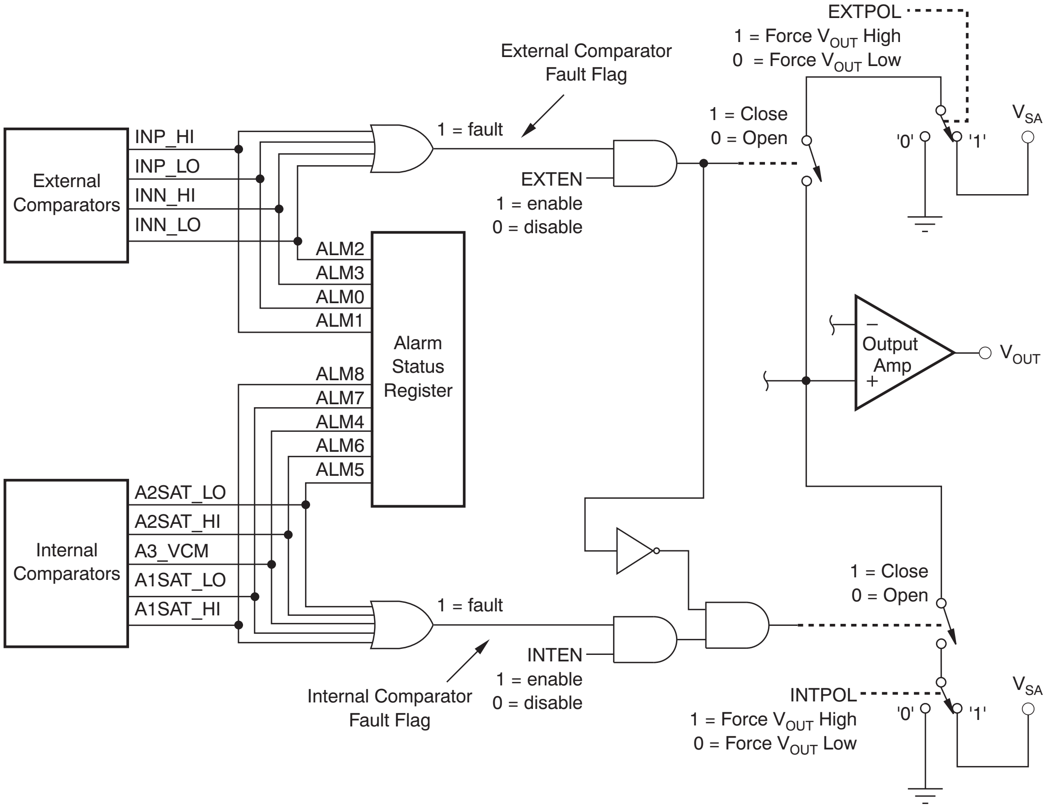


Figure 2-23. Fault Monitor Comparator Logic

Configuration for the fault monitor comparator logic is provided in Register 5—PGA Configuration and Over/Under Scale Limit. The individual comparator outputs in each group are combined to generate an Internal Comparator Fault flag and an External Comparator Fault flag. For the External Comparator group, EXTEN, Register 5 (bit 11) enables or disables whether the External Comparator Fault flag will be sent forward to force V_{OUT} to a fault indication state. For the Internal Comparator group, INTEN, Register 5 (bit 10), enables or disables whether the Internal Comparator Fault flag will be sent forward to force V_{OUT} to a fault indication state. For each of the comparator groups, there is programmability of the fault indication state on V_{OUT} (either V_{SA} or GND). INTPOL, Register 5 (bit 8), selects this state for the Internal Comparator group and EXTPOL, Register 5 (bit 9) selects for the External Comparator group. The External Comparator Fault flag has priority over the Internal Comparator.

Fault flag, as shown in Figure 2-23. For example, if the Internal Fault Comparator group is set to force V_{OUT} low and the External Fault Comparator group is set to force V_{OUT} high, and both groups detect a fault (which is possible if both are enabled), then the External Fault Comparator group prevails and V_{OUT} is forced high. This is to ensure that for most real-world applications, a critical sensor fault would be reported as priority over an internal node violation. Assuming there is a valid linear output on V_{OUT} at the time of a detected fault, the fault logic always prevails (if enabled), and will override the linear output to indicate a fault on V_{OUT} as positive or negative V_{OUT} saturation.

2.9 Over/Under Scale

The Over-Scale and Under-Scale Limit circuit provides a programmable upper and lower clip limit for the PGA309 output voltage. This circuit can be enabled by setting Register 5, bit D6 to ‘1’. When combined with the Fault Monitor circuitry, system diagnostics can be performed to determine if a conditioned sensor is defective or if the process being monitored by the sensor is out of range. Figure 2-24 details the key sections of the Over-Scale and Under-Scale Limit circuit. The selected PGA309 V_{REF} is divided down by a precision resistor string to form the over-scale and under-scale thresholds, as shown in Table 2-18 and

Table 2-19. Register 5 bits [5:0] set the desired thresholds. These resistor ratios are extremely accurate and produce no significant initial or temperature errors. As shown in Figure 2-24, there are two separate comparators: over-scale and under-scale, which use the over-scale or under-scale threshold, respectively, and determine where the PGA309 output (V_{OUT}) will be clipped. The dominant errors in the Over-Scale and Under-Scale Limit circuit are due to the comparators offset and offset temperature drift.

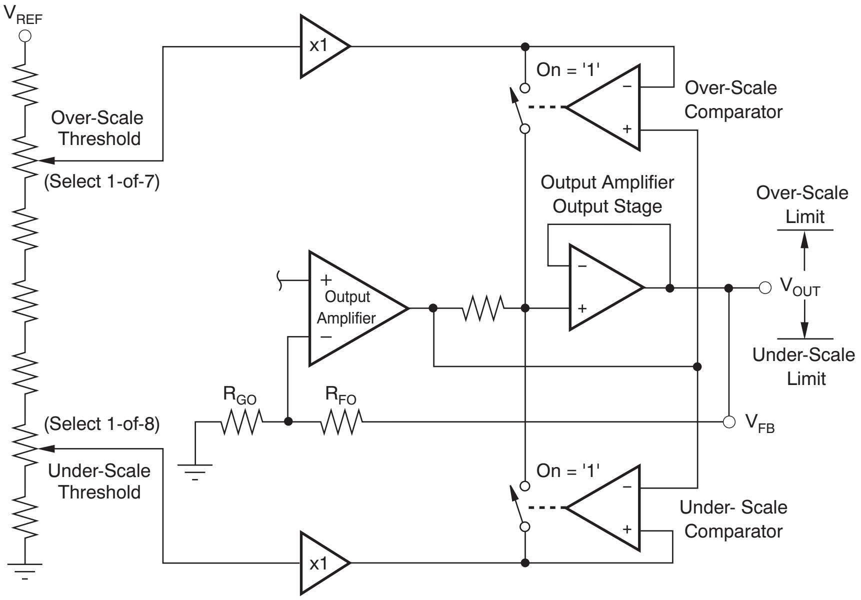


Figure 2-24. Over-Scale and Under-Scale Limit Circuit

Table 2-18. Over-Scale Threshold Selections (Register 5 Bits [5:3]). V_{REF} = +5V

HL2 [5]	HL1 [4]	HL0 [3]	Over-Scale Threshold (V)	Over-Scale Threshold
0	0	0	4.854	0.9708 V_{REF}
0	0	1	4.805	0.9610 V_{REF}
0	1	0	4.698	0.9394 V_{REF}
0	1	1	4.580	0.9160 V_{REF}
1	0	0	4.551	0.9102 V_{REF}
1	0	1	3.662	0.7324 V_{REF}
1	1	0	2.764	0.5528 V_{REF}
1	1	1	Reserved	—

Table 2-19. Under-Scale Threshold Selections (Register 5 Bits [2:0]). V_{REF} = +5V

LL2 [2]	LL1 [1]	LL0 [0]	Under-Scale Threshold (V)	Under-Scale Threshold
0	0	0	0.127	0.02540 V_{REF}
0	0	1	0.147	0.02930 V_{REF}
0	1	0	0.176	0.03516 V_{REF}
0	1	1	0.196	0.03906 V_{REF}
1	0	0	0.225	0.04492 V_{REF}
1	0	1	0.254	0.05078 V_{REF}
1	1	0	0.274	0.05468 V_{REF}
1	1	1	0.303	0.06054 V_{REF}

The design considerations in using the Over-Scale and Under-Scale Limit circuit are best understood through a definition by example, as shown in Example 2-4.

Example 2-4. Over/Under-Scale Calculation

Given:

Absolute Scale System—PGA309 connected to a system ADC (see Figure 2-25)
System ADC Reference: V_{REF} ADC = 4.096V
PGA309 Reference: V_{REF} = 4.096V (use PGA309 internal reference)
Operating Temperature Range: −40°C to +125°C
PGA309 V_{SA}, V_{SD} = +5V
External Fault Monitor; Trip High when Fault Detected

Find:

Recommended levels to allow for Over/Under-Scale Limits as well as Fault Detection.

(A) Over-Scale Limit

(B) Under-Scale Limit

(C) Useable Linear PGA309 Output Range

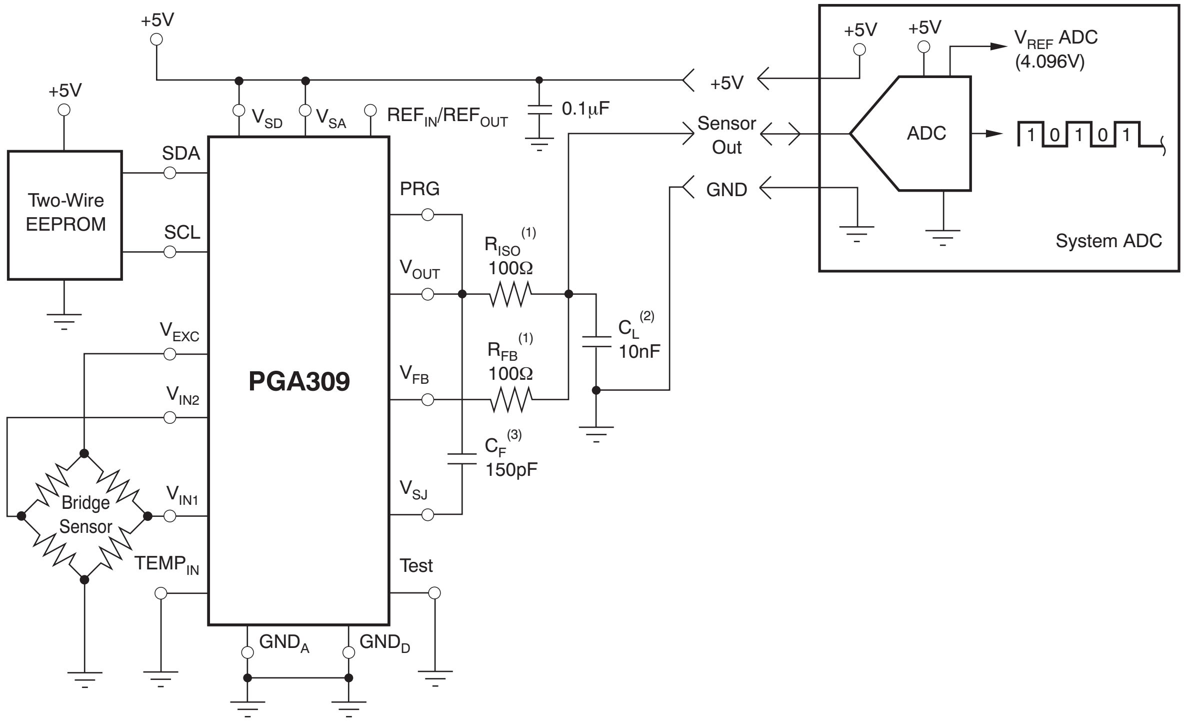
(D) System ADC Trip Points: Over-Scale, Under-Scale, Fault Detect

Solution:

1. Analyze the worst case offset errors on the over-scale and under-scale comparators over the operating temperature range. Table 2-20 contains key electrical characteristics needed for this computation.
   Over-Scale Comparator Offset Calculation:
   Over-Scale Temperature Drift:
   −40°C to 25°C: −24.05mV = (+0.37mV/°C)(−40°C − 25°C)
   25°C to +125°C: +37.00mV = (+0.37mV/°C)(+125°C − 25°C)
   Over-Scale Offset Min and Max:
   $V_{OS\ min}$ = +6mV −24.05mV = −18.05mV
   $V_{OS\ max}$ = +114mV + 37.00mV = +151.00mV
   Under-Scale Comparator Offset Calculation:
   Under-Scale Temperature Drift:
   −40°C to 25°C: +9.75mV = (−0.15mV/°C)(−40°C − 25°C)
   25°C to +125°C: −15.00mV = (−0.15mV/°C)(+125°C − 25°C)
   Under-Scale Offset Min and Max:
   $V_{US\ min}$ = −7mV + 9.75mV = −2.75mV
   $V_{US\ max}$ = −93mV −15.00mV = −108mV
2. Analyze the worst-case change in V_{REF} over the operating temperature range.
   V_{REF} Temperature Drift:
   −40°C to +125°C: [(+10ppm/°C)/(1e6)][+125°C − (−40°C)]V_{REF} = +0.00165 V_{REF}
   V_{REF} Min and Max:
   V_{REF} min = 4.00V – (0.00165)(4.00V) = 3.9934V
   V_{REF} max = 4.14V + (0.00165)(4.00V) = 4.1466V
3. Calculate the over-scale and under-scale min and max trip points over the operating temperature range for each overscale and under-scale threshold (refer to Table 2-21).
   Over-Scale (OS) Min and Max Trip Points:
   OS min = V_{REF} min (OS ratio) + $V_{OS\ min}$
   OS max = V_{REF} max (OS ratio) + $V_{OS\ max}$
   Under-Scale (US) Min and Max Trip Points:
   US min = V_{REF} min (US ratio) + $V_{US\ max}$
   US max = V_{REF} max (US ratio) + $V_{US\ min}$
4. From the over-scale and under-scale min and max trip point calculations, choose the best selection that will allow for the optimum system ADC range budget (see Figure 2-26). For this example, the PGA309 is scalable for a linear output of 8% to 80.8% of the system ADC reference. In addition, we can set reasonable trip points for detecting over-scale limit, under-scale limit, and fault detect.
5. Check that the PGA309 V_{OUT} can support the voltage swings defined in the System ADC range budget. Table 2-22 confirms that for our example the PGA309 V_{OUT} can meet the limiting conditions for our desired scaling.

Example 2-4. Over/Under-Scale Calculation (continued)

Since the PGA309 + sensor is usually calibrated together as a system, the over-scale and under-scale limits can be measured per device at the operating temperature extremes, and the final limits adjusted as desired for optimum scaling. In a ratiometrically scaled system, the reference error will not need to be included in the over-scale and under-scale trip point calculations.



NOTE: (Although not needed in all applications):

1. R_{ISO} and R_{FB} provide the PGA309 with overvoltage protection on Sensor Out.
2. C_L provides EMI/RFI filtering.
3. C_F provides the PGA309 with stability for capacitive load of C_L.

Figure 2-25. Absolute Scale System—PGA309 Connected to a System ADC

Table 2-20. Electrical Characteristics for Over-Scale and Under-Scale Comparators and V_{REF}

Parameter	Min	Typ	Max	Units
Over-Scale Comparator Offset	+6	+60	+114	mV
Over-Scale Comparator Offset Drift		+0.37		mV/°C
Under-Scale Comparator Offset	−7	−50	−93	mV
Under-Scale Comparator Offset Drift		−0.15		mV/°C
V_{REF2}	4.00	4.096	4.14	V
V_{REF2} Drift		+10		ppm/°C

Table 2-21. Over-Scale and Under-Scale Min and Max Trip Point Calculations(1)

Threshold U = Under-Scale O = Over-Scale	Threshold Ratio to V_{REF}	Min Trip (V)	Min Trip (%V_{REF} ADC)	Max Trip (V)	Max Trip (%V_{REF} ADC)	Typ Trip (V)	Typ Trip (%V_{REF} ADC)
U7	0.0605	0.1338	3.2656	0.2483	6.0616	0.1910	4.6636
U6	0.0547	0.1104	2.6943	0.2240	5.4684	0.1672	4.0814
U5	0.0508	0.0948	2.3141	0.2078	5.0736	0.1513	3.6938
U4	0.0449	0.0714	1.7428	0.1835	4.4804	0.1274	3.1116
U3	0.0391	0.0480	1.1714	0.1592	3.8871	0.1036	2.5293
U2	0.0352	0.0324	0.7912	0.1430	3.4923	0.0877	2.1418
U1	0.0293	0.0090	0.2199	0.1187	2.8991	0.0639	1.5595
U0	0.0254	−0.0066	−0.1603	0.1026	2.5042	0.0480	1.1719
O6	0.5528	2.1895	53.4546	2.4432	59.6494	2.3164	56.5520
O5	0.7324	2.9067	70.9648	3.1880	77.8313	3.0473	74.3980
O4	0.9102	3.6167	88.2994	3.9252	95.8309	3.7710	92.0652
O3	0.9160	3.6399	88.8649	3.9493	96.4181	3.7946	92.6415
O2	0.9394	3.7333	91.1462	4.0463	98.7870	3.8898	94.9666
O1	0.9610	3.8196	93.2521	4.1359	100.9737	3.9777	97.1129
O0	0.9708	3.8587	94.2076	4.1765	101.9658	4.0176	98.0867

(1) $V_{REF\ MIN} = 3.9934V$, $V_{REF\ MAX} = 4.1466V$, V_{REF} ADC = 4.096V, $V_{OS\ min} = -0.01805V$, $V_{OS\ max} = 0.151V$, $V_{US\ min} = -0.00275V$, $V_{US\ max} = -0.108V$. Bold Italics indicate final choice for Example 2-4.

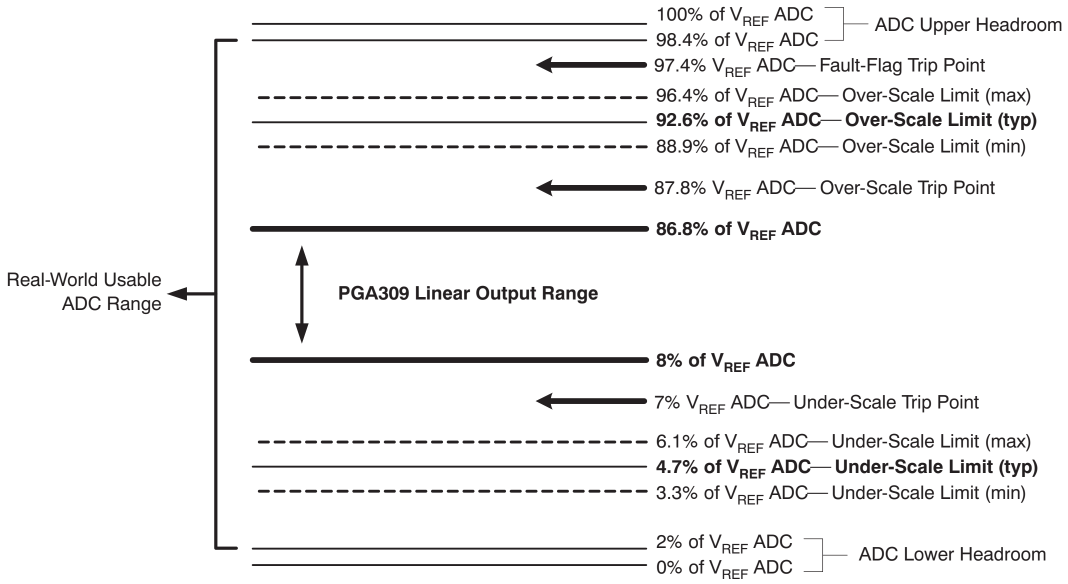


Figure 2-26. System ADC Range Budget for Over-Scale, Under-Scale, and Linear Output

Table 2-22. PGA309 V_{OUT} Limits for System ADC Range Budget(1)

Limiting Condition	PGA309 V_{OUT} (V)	PGA309 V_{OUT} Limit (V)
96.4% V_{REF} ADC—Over-Scale Limit (max)	3.9493	4.9
3.3% V_{REF} ADC—Under-Scale Limit (min)	0.1338	0.1

(1) V_{REF} ADC = 4.096V, V_{SA} = 5V.

2.10 Noise and Coarse Offset Adjust

The PGA309 Front-End PGA contains auto-zero operational amplifiers that allow precision, low-noise measurements free from flicker, or 1/f noise, that is typically present in regular low-voltage CMOS op amps.

This auto-zero topology operates by canceling amplifier low-frequency noise and offset during each clock cycle of an internal oscillator. This flattens the lowfrequency noise voltage spectrum of the PGA309, leaving only a small residual clock feedthrough component at ~7kHz and its multiples. Figure 2-27 details the PGA309 voltage noise spectrum for coarse offset adjust = 0mV. This auto-zero method allows higher precision measurement by filtering the output of the PGA309 proportionally. Conventional CMOS operational amplifiers that use averaging do not improve the signal-to-noise ratio in the 1/f noise region. In addition, the auto-zero technique allows the PGA309 input offset voltage to achieve very good temperature and time stability.

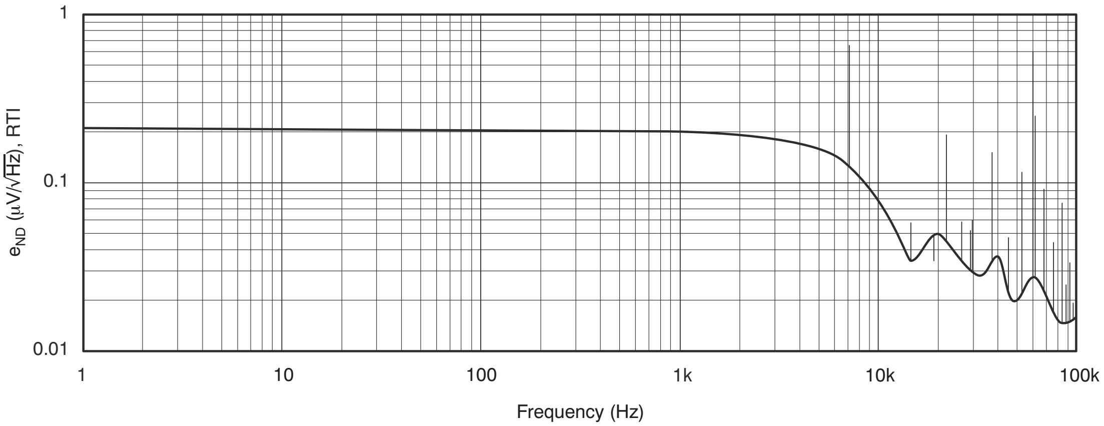


Figure 2-27. Voltage Noise Power Spectrum Referred to Input (RTI), Coarse Offset Adjust = 0mV, Gain = 1152, CLK_CFG = ‘00’ (default)

The PGA309 low-frequency voltage noise density (RTI) is ~210nV/$\sqrt{\text{Hz}}$. To convert this to a peak-to-peak amplitude for oscilloscope measurements, the following equation is supplied:

$V_{NPP} = (e_{ND})(\sqrt{BW})(\text{crest factor})$

where:

- V_{NPP} = voltage noise peak-to-peak (nV_{PP})
- e_{ND} = voltage noise density (nV/$\sqrt{\text{Hz}}$)
- BW = bandwidth of interest (Hz)
- Crest Factor = probability factor for conversion of rms noise to peak-topeak noise (crest factor of 6 reduces probability of seeing a larger peak-topeak amplitude to < 0.3%).

PGA309 peak-to-peak noise, RTI, BW = 10Hz:

$V_{NPP} = (210\text{nV}/\sqrt{\text{Hz}})(\sqrt{10\text{Hz}})(6) = 3984\text{nV}_{PP} = 3.98\mu\text{V}_{PP}$ (RTI)

For a PGA309 total gain of 1152, this implies the noise at V_{OUT} will be 4.58mV_{PP} , as shown in Figure 2-28.

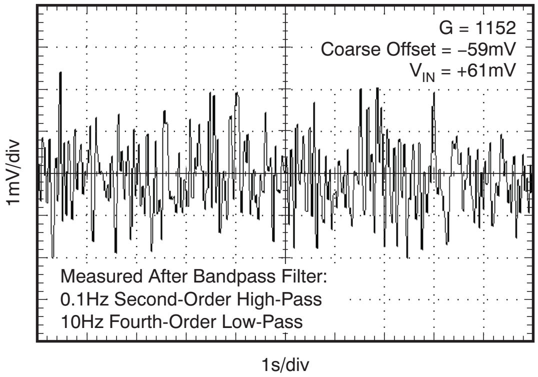


Figure 2-28. V_{OUT} Noise, 0.1Hz to 10Hz Peak-to-Peak Noise

To compensate for bridge sensors with a large initial offset, the input stages of the PGA309 Front-End PGA incorporate a patented circuit for the coarse offset adjust based on the auto-zero topology. For each clock cycle of the internal auto-zero oscillator, the offsets and noise of the input amplifier stages are subtracted from the input signal, and the result is summed with a small voltage produced by the Coarse Offset Adjust DAC. This resulting value becomes the input-referred offset of the PGA309. This value can be positive or negative as described Section 2.2, *Offset Scaling*. This operation does not increase the low frequency 1/f noise of the PGA309. However, the mismatches of internal elements in the Coarse Offset DAC can produce temperature and long-term stability errors on the same order of magnitude as regular, traditional CMOS op amps (that is, temperature drift of input offset voltage of up to 10µV/°C).

To produce a value that is temperature- and time-stable, the Coarse Offset DAC circuitry incorporates a chopping circuit that rotates internal components, averaging the mismatch error on the output of the Coarse Offset Adjust DAC. This produces a very time- and temperature-stable coarse offset adjust.

The design compromise of the Coarse Offset DAC chopping technique is a clock feedthrough glitch that can be seen at V_{OUT}, the output of the PGA309, due to the rotating elements. With the Coarse Offset Adjust set to 0mV the clock feedthrough components are practically negligible on the V_{OUT} signal of the PGA309, as shown in Figure 2-29.

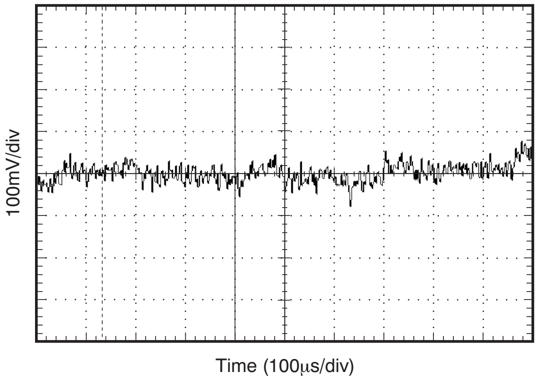


Figure 2-29. Unfiltered V_{OUT} Clock Feedthrough, Coarse Offset Adjust = 0mV, Gain = 1152, CLK_CFG = ‘00’ (default)

As the Coarse Offset Adjust DAC value increases the amplitude of the clock, feedthrough glitch also increases. For V_{REF} = +5V and a full-scale Coarse Offset DAC value of −59mV, the clock feedthrough glitch is shown in Figure 2-30. This scope photo is for the PGA309 set in its maximum internal gain of 1152, with the Coarse Offset Adjust DAC set to −59mV and V_{IN} set to +61mV. Referred to input (RTI), this V_{OUT} glitch is only 347µV_{PP} (0.4V_{PP}/1152). This glitch occurs at half of the internal auto-zero clock; typically, 3.5kHz. This glitch does not reflect back into the low-frequency range and can be filtered out if the signal of interest is at or below 1kHz. Figure 2-31 is a scope photo of V_{OUT} peak-to-peak noise for this case. Figure 2-32 shows the voltage noise spectrum for the case where the Coarse Offset Adjust DAC is set to −59mV and V_{IN} = +61mV. In Figure 2-32, the baseband noise is about the same as when the coarse offset adjust was set to zero, as in Figure 2-27, but with an additional spike at about 3.5kHz.

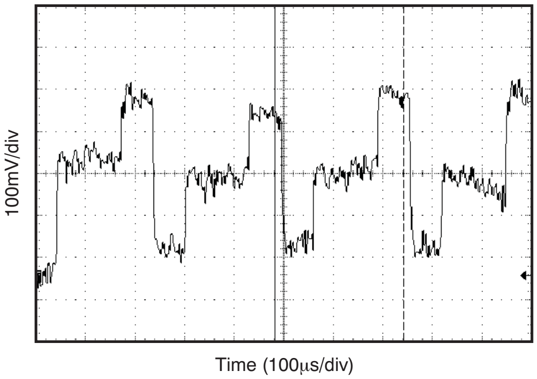


Figure 2-30. Unfiltered V_{OUT} Clock Feedthrough Glitch, Coarse Offset Adjust = −59mV, Gain = 1152, V_{IN} = +61mV, CLK_CFG = ‘00’ (default). V_{OUT} Glitch (RTI) = 347µV_{PP}

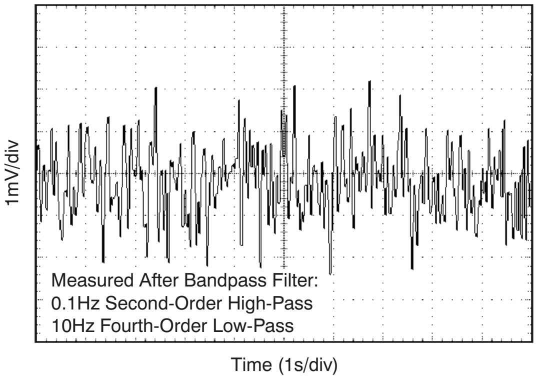


Figure 2-31. Filtered 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise, Coarse Offset Adjust = −59mV, Gain = 1152, V_{IN} = +61mV, CLK_CFG = ‘00’ (default)

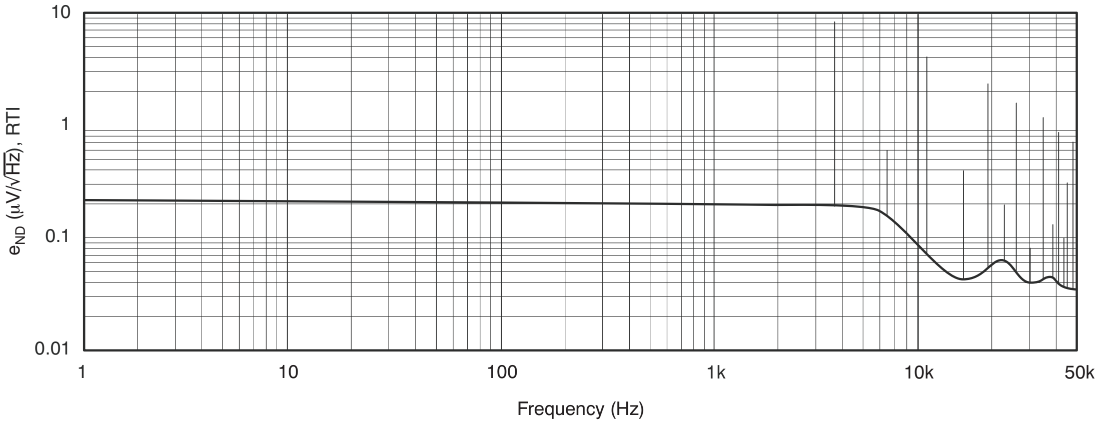


Figure 2-32. Voltage Noise Spectrum (RTI), Coarse Offset Adjust = −59mV, Gain = 1152, V_{IN} = +61mV, CLK_CFG = ‘00’ (default)

For applications where the clock feedthrough glitch from the Coarse Offset Adjust DAC chopping circuitry is an issue, there are alternate modes that can be selected for the Coarse Offset DAC clocking and the auto-zero clocking of the Front-End PGA. Register 5 bits (13:12) are referenced as CLK_CFG1 and CLK_CFG0, respectively. Table 2-23 outlines the clocking schemes available using these bits. Up to this point, CLK_CFG = ‘00’ has been discussed.

Table 2-23. PGA309 Clocking Schemes

CLK_CFG Mode	CLK_CFG1 Bit D13	CLK_CFG0 Bit D12	Auto-Zero PGA Front-End	Chopping Coarse Offset DAC
00 (default)	0	0	7kHz typical	3.5kHz typical
01	0	1	7kHz typical	Off (none)
10	1	0	7kHz typical, Random Clocking	3.5kHz typical, Random Clocking
11	1	1	7kHz typical	3.5kHz typical, Random Clocking

In the CLK_CFG = ‘01’ mode, the Coarse Offset Adjust DAC chopping is turned off. The clock feedthrough glitch is no longer present (Figure 2-33 shows the 0.1Hz to 10Hz V_{OUT} peak-to-peak noise) and the V_{OUT} noise spectrum is clean, as shown in Figure 2-34. However, the input Coarse Offset Adjust DAC is no longer temperature-stable. Typical span drift is generally linear with temperature and may be acceptable in applications where the PGA309 is located close to the bridge sensor and they are both calibrated together. The drift of the Coarse Offset Adjust DAC simply sums with the bridge sensor offset drift, and they are both calibrated out.

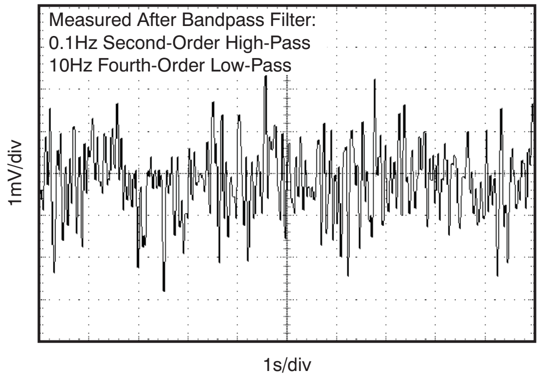


Figure 2-33. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = ‘01’, V_{NPP} (RTI) = 4.44 V_{PP}

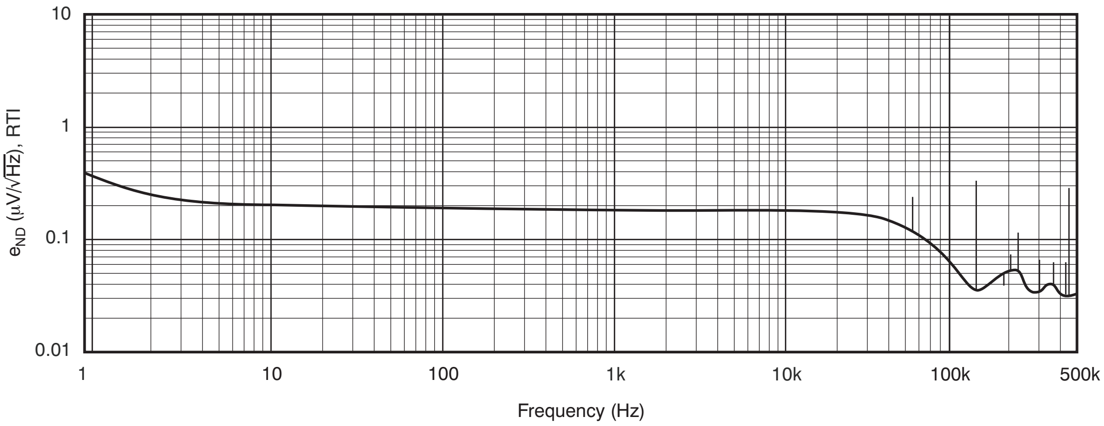


Figure 2-34. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = ‘01’

CLK_CFG = ‘10’ mode and CLK_CFG = ‘11’ mode turn on different clock randomization schemes for the Front-End PGA auto-zero and Coarse Offset DAC chopping. Although this does not reduce the amplitude of the clock feedthrough glitch (see Figure 2-30), it does spread the glitch energy over a wider frequency range. This removes the fixed spike at half of the input auto-zero clock frequency, but raises the noise floor in the lower frequency range, thus increasing the baseband noise. CLK_CFG = ‘11’ mode simply whitens the peak-to-peak noise from the 1Hz region to about the 7kHz region by modulating both the auto-zero and chopping clocks. In CLK_CFG = ‘10’ mode, the Coarse Offset DAC chopping clock is modulated but not the auto-zero clock. The results of these two modes are shown in both voltage noise spectrum and peak-to-peak noise plots in Figure 2-35, Figure 2-36, Figure 2-37, and Figure 2-38.

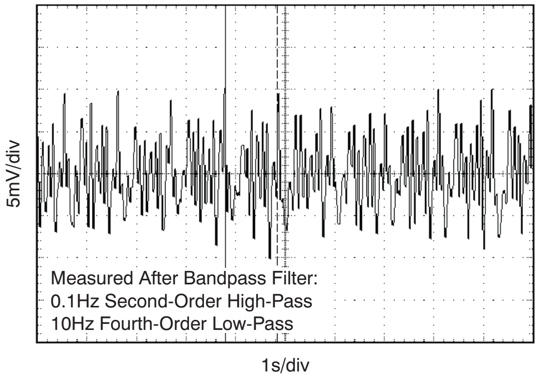


Figure 2-35. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = ‘10’, V_{NPP} (RTI) = 18.4µV_{PP}

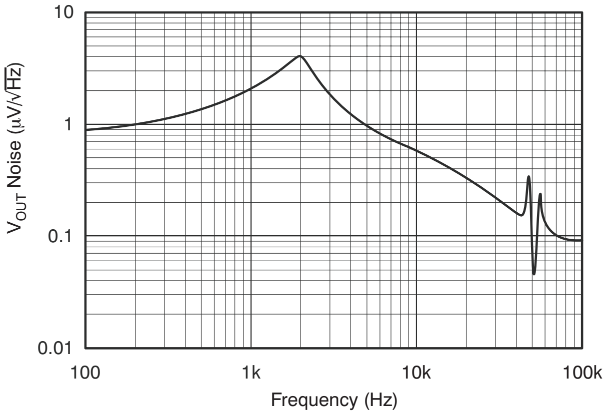


Figure 2-36. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = ‘10’

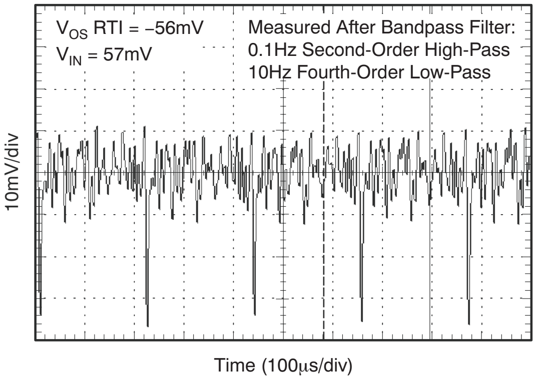


Figure 2-37. 0.1Hz to 10Hz V_{OUT} Peak-to-Peak Noise for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = ‘11’, V_{NPP} (RTI) = 42µV_{PP}

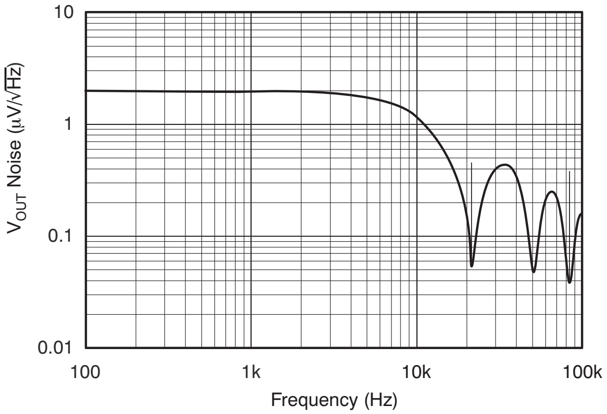


Figure 2-38. V_{OUT} Noise Spectrum for Coarse Offset Adjust = −56mV, Gain = 1152, V_{IN} = +57mV, CLK_CFG = ‘11’

2.11 General AC Considerations

In addition to normal good analog layout and design practices, there are a few key items to check when designing with the PGA309.

1. REFIN/REFOUT, pin 16: Keep capacitive loading to 200pF or less.
2. V_{EXC}, pin 1: Keep capacitive loading to 200pF or less.
3. V_{SA}, pin 3 and V_{SD}, pin 10: Keep these within 200mV of each other. Internally, the PGA309 separates its digital and analog power supplies to minimize cross-talk between the two. Externally, tie the two together and bypass, directly at the pins, with a 0.1µF capacitor. If an RC filter is used between the two supplies, ensure that maximum drop is never more than 200mV.
4. GND_A, pin 2 and GND_D, pin11: Ensure that these are both tied directly together and connected to the same ground point.
5. V_{SJ}, pin 8: This is the negative input to the Output Amplifier and as such, it is high-impedance. Route low-impedance traces, such as V_{OUT}, and noisy traces away from V_{SJ}. Minimize trace lengths to avoid unwanted additional capacitance on V_{SJ}.
6. V_{IN1}, pin 4 and V_{IN2}, pin 5: For source resistances greater than or equal to 10kΩ, add a capacitor of 1nF to 2nF between V_{IN1} and V_{IN2} to minimize noise coupling.
7. V_{IN1}, pin 4 and V_{IN2}, pin 5: RFI filtering is always a concern for instrumentation amplifier applications. RFI signals injected into instrumentation amplifiers become rectified and appear on the output as a DC drift or offset; high-gain circuits amplify this effect. Figure 2-39 depicts input filtering for the PGA309. Depending upon the distance of the bridge sensor from the PGA309 and the sensor module shielding, R1 and R2 may be required. C1 should be equal to C2, and C3 should be ten times larger than C1 to attenuate any common-mode signals that become differential due to the mismatch in C1 and C2. All input filter components should be located directly at the PGA309 inputs to avoid and trace lengths from becoming receiving RFI antennas.

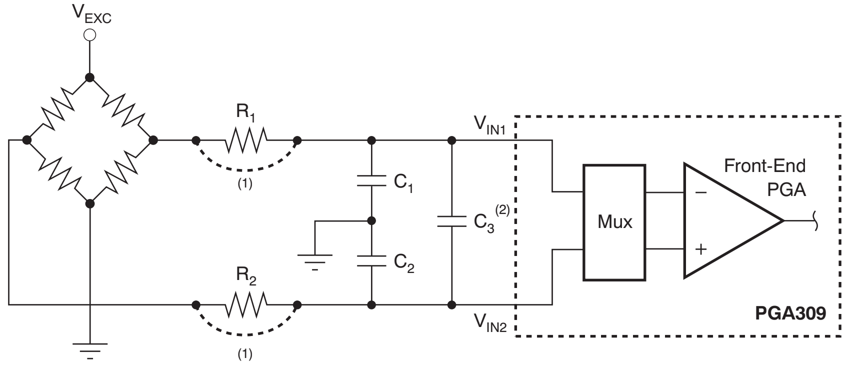


Figure 2-39. Input Filtering

Operating Modes

This chapter describes the operating modes of the PGA309.

Topic **Page**

3.1 Power-On Sequence and Normal Stand-Alone Operation

The PGA309 internal state machine controls the operations of the part in Stand-Alone Mode, without any external digital controller. In this mode, the PGA309 performs the functions of a Two-Wire interface master to read the data from the EEPROM.

The PGA309 has power-on reset (POR) circuitry to reset the internal registers and subcircuits to their initial states. This power-on reset also occurs when the supply is detected to be too low so that the PGA309 is in a known state when the supply becomes valid again. The threshold for the POR circuit is typically 2.2V for V_{SA} rising and 1.7V for V_{SA} falling.

After the power supply becomes valid, the PGA309 waits for approximately 33ms and then attempts to read the configuration register data (Register 3—Register 6 bit settings) from the first part of the external EEPROM device. If the EEPROM has the proper programmed flag word (0x5449, “TI” ASCII) in address locations 0 and 1, the PGA309 will continue reading the EEPROM. Otherwise, the PGA309 will wait for 1.3 seconds before trying again. If the PGA309 detects that there was no response from the EEPROM and the TwoWire bus was in a valid idle state (SCL = ‘1’, SDA = ‘1’), then the PGA309 will wait for 1.3 seconds and try again. If the Two-Wire bus is stuck with SDA = ‘0’, the PGA309 will try to free the bus by sending extra clocks down SCL (see Chapter 4, *Digital Interface*, for details), and wait for 33ms before trying to read the EEPROM again. If the EEPROM configuration read is successful (including valid Checksum1 data) and either bits ADCS or CEN in Register 6 are set to ‘1’, the PGA309 will trigger the Temp ADC to measure the temperature information as configured in the configuration registers. For 16-bit resolution results, the converter takes approximately 125ms to complete a conversion. Once the conversion is complete, the PGA309 begins reading the Lookup Table from EEPROM address locations 16 and higher, to calculate the settings for the Gain and Zero DACs using the piecewise linear interpolation algorithm. The PGA309 reads the entire Lookup Table and determines if the checksum for the Lookup Table (Checksum2) is correct. Each entry in the Lookup Table requires approximately 500μs to read from the EEPROM. Once Checksum2 is determined to be valid, the calculated value for the Gain and Zero DACs is updated into their respective registers, and the Output Amplifier (V_{OUT}) is enabled. The PGA309 then begins looping through this entire procedure, starting again with reading the configuration data from the first part of the EEPROM. This loop continues indefinitely.

NOTE: For PRG Pin Connected to V_{OUT}

During the entire initial power-on sequence, the PGA309 V_{OUT} is disabled (high-impedance) until valid EEPROM contents are verified and an ADC conversion is complete, as described above and illustrated in Figure 3-1. In true three-wire connection (VS, GND, and V_{OUT} with PRG pin shorted to V_{OUT}), with OWD = ‘1’ (Register 4, bit D15), the time interval after power-up is the only opportunity that an external communications controller can initiate digital communication with the PGA309 and trigger a one second delay in the internal state machine. After V_{OUT} is enabled no further digital communication is possible, unless power is cycled.

If the PGA309 detects that there is no EEPROM device present (that is, it does not receive an acknowledge to a slave address byte sent to the EEPROM), the PGA309 will wait for approximately one second and try again. It will continue in this loop indefinitely with V_{OUT} disabled.

At any time, if the PGA309 is addressed through the Two-Wire or One-Wire interface with OWD = ‘0’ (Register 4, bit D15), the internal state machine aborts its cycle and initiates a 1s delay. After the 1s delay has timed out, a EEPROM read is started. The 1s delay is reset every time the PGA309 is addressed. This allows an external microcontroller to control the function of the PGA309, as long as some communication activity is addressed to the PGA309 at least once per second. V_{OUT} will stay in the state (enabled or disabled) that it was in before the PGA309 was addressed. If full microcontroller control of the PGA309 is desired from initial power-on, then the Test pin should be brought high to enable the output after the internal PGA309 registers have been configured to their desired states.

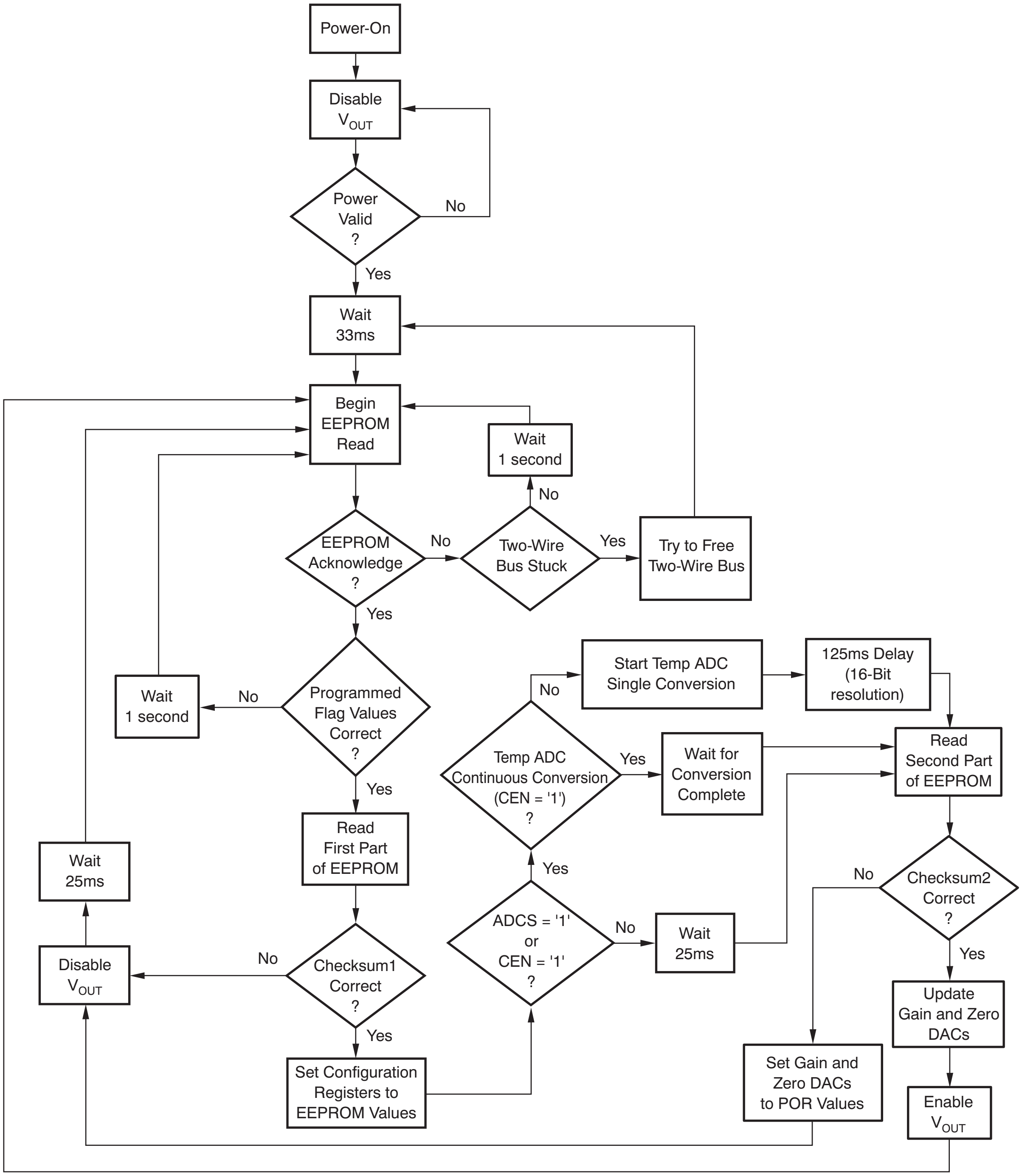


Figure 3-1. State Machine—Power-On Sequence and Operation in Stand-Alone Mode

3.2 EEPROM Content and Temperature Lookup Table Calculation

The PGA309 uses an industry standard, Two-Wire, external EEPROM (typically, a SOT23 package). A 1k-bit minimum EEPROM is needed if all 17 temperature coefficients are used. Larger EEPROMs may be used to provide additional user space for serial number, lot code, or other product data.

The 16-bit data words used by the PGA309 are stored in the external EEPROM, least significant 8-bit byte first, as shown in Figure 3-2.

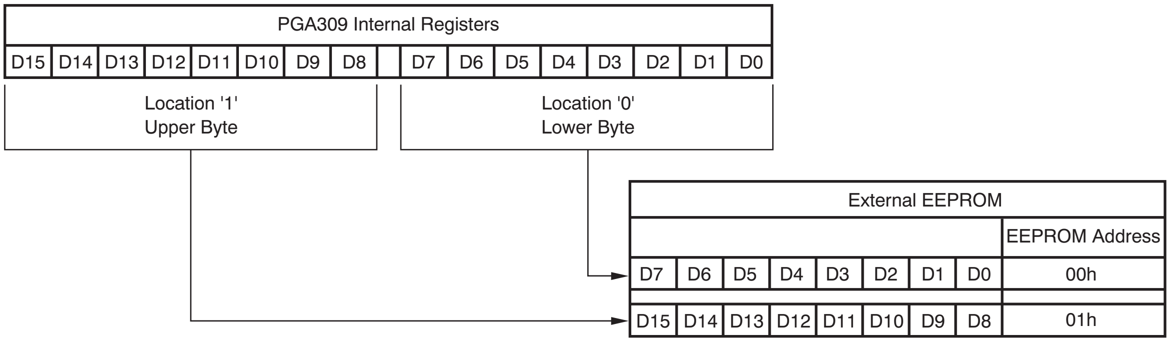


Figure 3-2. PGA309 Internal Registers Map to External EEPROM Addresses

Table 3-1 outlines the external EEPROM contents for a 1k−bit EEPROM. For a detailed External EEPROM Example refer to Appendix A.

The first part of the EEPROM (16 8-bit bytes), address location 1/0 through address location 15/14, contains the EEPROM Programmed Flag and the PGA309 configuration data for Registers 3, 4, 5, and 6. Included at the end of this section is Checksum1, at address location 15/14.

The second part of the EEPROM (108 8-bit bytes), address location 17/16 through address location 123/122, contains the temperature coefficient Lookup Table for the Zero DAC (Fine Offset Adjust) and Gain DAC (Fine Gain Adjust). There can be up to 17 temperature index values with corresponding scale factors for the Gain DAC and Zero DAC. The temperature values in the Lookup Table represent points on the piecewise linear curves that compensate for sensor span and offset temperature drifts. Each temperature value corresponds to respective slope factors for the Gain DAC and Zero DAC. The DAC values are linearly interpolated for a measured temperature that does not fall directly on a stored temperature value.

Table 3-1. 1k-Bit External EEPROM Contents

	EEPROM Address Location ‘1’ (Decimal)	EEPROM Address Location ‘0’ (Decimal)	Content (All data are stored as two 8-bit bytes)
First Part	1	0	EEPROM Programmed Flag; 5449h = “TI” ascii
	3	2	Not used, but include in Checksum1 calculation; available for user data.
	5	4	Not used, but include in the Checksum1 calculation; available for user data.
	7	6	Value for PGA309 Register 3, Reference Control and Linearization
	9	8	Value for PGA309 Register 4: PGA Coarse Offset and Gain/Output Amplifier Gain
	11	10	Value for PGA309 Register 5: PGA Configuration and Over/Under-Scale Limit
	13	12	Value for PGA309 Register 6: Temp ADC Control
	15	14	Checksum1= FFFFh − sum(hex values of location 1/0 thru 13/12) Checksum1 truncated above 16 bits
Second Part	17	16	T0 (Temperature Index Value for Temp ≤ T0)
	19	18	Z0 (Zero DAC Value for Temp ≤ T0)
	21	20	G0 (Gain DAC Value for Temp ≤ T0)
	23	22	T1 (Temperature Index Value T1)
	25	24	ZM1 (Zero DAC Multiplying Slope Factor for T1 ≤ Temp ≤ T0)
	27	26	GM1 (Gain DAC Multiplying Slope Factor for T1 ≤ Temp ≤ T0)
	...	...	...
	...	...	...
	...	...	...
	113	112	T16 (Temperature Index Value T1)
	115	114	ZM16 (Zero DAC Multiplying Slope Factor for T15 ≤ Temp ≤ T16)
	117	116	GM16 (Gain DAC Multiplying Slope Factor for T15 ≤ Temp ≤ T16)
	119	118	T_{END} (End of Lookup Table → 7FFFh)
	121	120	ZM_{END} (End of Lookup Table; value ignored but included in Checksum2)
	123	122	GM_{END} (End of Lookup Table; value ignored but included in Checksum2) Checksum2 = FFFFh − sum(Hex values of location 17/16 thru 123/122) Checksum2 truncated above 16 bits
	125	124	Not used; available for user data
	127	126	Not used; available for user data

T0, T1, T2 ... Tx (where $x \leq 16$) are the temperature index values in the Lookup Table. These are output results from the Temp ADC. The values must be monotonically increasing from minimum to maximum for the Lookup Table to function correctly. Note that this does not necessarily correspond to increasing temperature. For example, if a diode voltage is being measured by the Temp ADC, its readings will be decreasing with temperature. However, the Lookup Table must still be built from minimum Temp ADC reading to the maximum Temp ADC reading. The data format for Tx is 16-bit data with a format dependent upon which Temp ADC mode is selected (see Section 6.2.7, *Register 6: Temp ADC Control Register*).

Z0 is the value of the Zero DAC setting for temperatures T0 and below. Z0 data format is unsigned 16-bit data. The equation for the Zero DAC value is:

$$Zx = \left(\frac{V_{Zdesired}}{V_{REF}}\right) \bullet 65{,}536 \tag{13}$$

where $0 \leq Zx \leq 65535$ (programmable range) and $0.1V \leq \text{Zero DAC} \leq V_{SA} - 0.1V$ (analog limits).

G0 is the value of the Gain DAC setting for temperatures T0 and below. G0 data format is unsigned 16−bit data. The equation for the Gain DAC value is:

$$Gx = \left(\text{Gain}_{desired} - \frac{1}{3}\right) \bullet \frac{3}{2} \bullet 65{,}536 \tag{14}$$

where $0.3333333 \leq \text{Gain DAC} \leq 0.9999898$ and $0 \leq Gx \leq 65535$.

ZM1, ZM2 … ZMi are multiplying slope factors for each piecewise linear segment for the Zero DAC adjustment. They are calculated based on the desired values Z1, Z2 … Zx (calculated same as Z0) of the Zero DAC for T1, T2 … Tx respectively. The equation for calculating the ZMi slope factors is:

$$ZMi = 256\left[\frac{Zx - Z(x-1)}{Tx - T(x-1)}\right] \tag{15}$$

The ZMi scale factor of 256 is to format the decimal value for PGA309 internal binary arithmetic. These numbers are 16-bit, Twos Complement data format. See Table 3-2 for an example of the Lookup Table.

GM1, GM2 … GMi are multiplying slope factors for each piecewise linear segment for the Gain DAC adjustment. They are calculated based on the desired values G1, G2 … Gx (calculated the same as G0) of the Gain DAC for T1, T2, T3 …Tx, respectively. The equation for calculating the GMi slope factors is:

$$GMi = 256\left[\frac{Gx - G(x-1)}{Tx - T(x-1)}\right] \tag{16}$$

The GMi scale factor of 256 is to format the decimal value for PGA309 internal arithmetic. These numbers are 16-bit, Two's-Complement data format.

The end of the Lookup Table is flagged by temperature index value T_{END} = 7FFFh in the temperature index data. The ZM_{END} value of this entry is ignored but is included in Checksum2. The ZM_{END} value should be set to zero. The GM_{END} value of this entry becomes Checksum2, the checksum for the second part of the EEPROM.

Example 3-1 details the calculation of Lookup Table values and how the PGA309 lookup table linear interpolation algorithm works.

3.2.1 Temperature Lookup Table Calculation

Example 3-1. Temperature Lookup Table Calculation

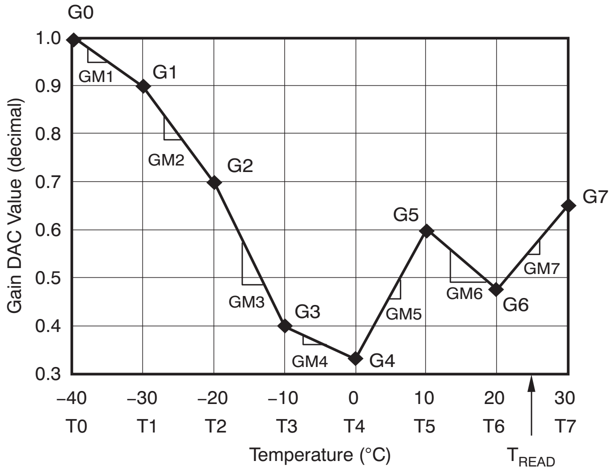
In Figure 3-3, G0−G7 are the exact desired settings at T0−T7, respectively, for the Gain DAC. GM1−GM7 are the slopes of the piecewise linear curves that connect G0 to G1, G1 to G2, G2 to G3, G3 to G4, G4 to G5, G5 to G6, and G6 to G7. This example demonstrates how the Lookup Table is constructed and how the Lookup Logic with Linear Interpolation Algorithm accurately calculates the setting for the Gain DAC at T_{READ} = 25°C. Note that T_{READ} = 25°C does not fall on an exact data point (Tx, Gx). Temperature coefficients for both the Gain DAC and the Zero DAC are calculated to complete the Lookup Table.

Given:

1. Desired Gain DAC values as in Figure 3-3 and Zero DAC values as in Figure 3-4.
2. Internal Temperature Mode with resolution set to 12-bit (16-bit data format: 12-bit, sign-extended, right-justified, Twos Complement).
3. V_{REF} = +5V.

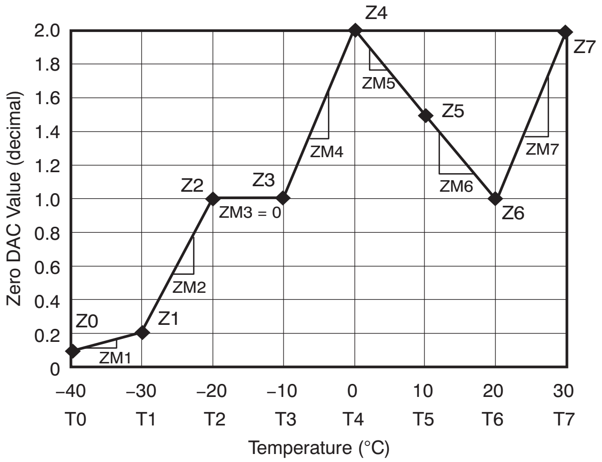
Find:

Gain DAC slope factors (GMi) and Zero DAC slope factors (ZMi).



Temp (°C)	Gain DAC
−40	1
−30	0.9
−20	0.7
−10	0.4
0	0.3333
10	0.6
20	0.4756
30	0.6543

Figure 3-3. Desired Gain DAC Values



Temp (°C)	Zero DAC
−40	0.1
−30	0.2
−20	1
−10	1
0	2
10	1.5
20	1
30	2

Figure 3-4. Desired Zero DAC Values

Step 1:

Calculate Temp ADC counts for the temperature range of interest using Table 3-2.

Table 3-2. Temp ADC Temperature vs Counts

Temperature (°C)	Temp ADC (Counts)	Temp ADC (Hex)
−40	−640	FD80
−30	−480	FE20
−20	−320	FEC0
−10	−160	FF60
0	0	0000
10	160	00A0
20	320	0140
25	400	0190
30	480	01E0

The resolution for the Temp ADC in Internal Temperature Mode is 0.0625°C/count.

For positive temperatures (for example, 20°C):

(20°C)/(0.0625°C/count) = 320 → 140h → 0001 0100 0000

Twos Complement is not performed on positive numbers. Simply convert the number to binary code with 16-bit, right-justified format, and MSB = ‘0’ to denote a positive sign. Extend the sign to the upper 4 bits.

20°C will be read by the Temp ADC as 0000 0001 0100 0000 → 140h

For negative temperatures (that is, −20°C):

(|−20|)/(0.0625°C/count) = 320 → 140h → 0001 0100 0000

Generate the Twos Complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by MSB = ‘1’. Extend the sign to the upper 4 bits to form the 16-bit word.

−20°C will be read by the Temp ADC as 1111 1110 1100 0000 → FEC0h.

Step 2:

Calculate Gain DAC temperature coefficients using Table 3-3.

For the Gain DAC desired counts (that is, G3 = 0.4):

Gx = (GainDESIRED − 1/3)(3/2)(65536)
G3 = (0.4 − 1/3)〈3/2)(65536) = 6553.6
0 ≤ Gx ≤ 65535
0.3333333 ≤ Gain DAC ≤ 0.9999898

For positive slopes (that is, GM5):

GM5 = [(G5 − G4)/(T5 − T4)][256]
GM5 = [(26214.4 − 0)/(160 − 0)][256] = 41943.04
Integer [41943.04] = 41943
GM5 = 41943 → A3D7h → 1010 0011 1101 0111

For negative slopes (that is, GM2):

GM2 = [(G2 − G1)/(T2 − T1)][256]
GM2 = [(36044.8 − 55705.6)/(−320 − {−480})][256] = −31457.28
Integer [−31457.28] = −31457
Generate the Twos Complement of −31457:
GM2 = 851Fh → 1000 0101 0001 1111

NOTE: Gain DAC Slopes

If the Gain DAC slope computes to a count > 65535, there is a problem. The Temp ADC must be reconfigured for lower resolution or the number of points in the Lookup Table must be increased to bring the slopes within the PGA309 computation region.

Table 3-3. Gain DAC Temperature Coefficient Calculation

Temp (°C)	Temp Index	Temp ADC (Counts)	Gain DAC Desired Value	Gain DAC Desired Index	Gain DAC Desired (Counts)	Gain DAC Slope	Gain DAC Slope Formula	Gain DAC Slope [1] (Counts)	Gain DAC Slope (Hex)
−40	T0	−640	1	G0	65535	G0	G0 = G0	65535	FFFF
−30	T1	−480	0.9	G1	55705.6	GM1	GM1 = [(G1 − G0)/T1 − T0)][256]	−15727	C291
−20	T2	−320	0.7	G2	36044.8	GM2	GM2 = [(G2 − G1)/T2 − T1)][256]	−31457	851F
−10	T3	−160	0.4	G3	6553.6	GM3	GM3 = [(G3 − G2)/T3 − T2)][256]	−47104	4800
0	T4	0	0.3333	G4	0	GM4	GM4 = [(G4 − G3)/T4 − T3)][256]	−10496	D700
10	T5	160	0.6	G5	26214.4	GM5	GM5 = [(G5 − G4)/T5 − T4)][256]	41943	A3D7
20	T6	320	0.4756	G6	13985.4	GM6	GM6 = [(G6 − G5)/T6 − T5)][256]	−19566	B392
30	T7	480	0.6543	G7	31552.3	GM7	GM7 = [(G7 − G6)/T7 − T6)][256]	28107	6DCB

[1] Integer [Gain DAC Slope Formula].

Step 3:

Calculate Zero DAC temperature Coefficients using Table 3-4.

For the Zero DAC desired counts (for example, Z5 = 1.5):

$Zx = (V_{ZDESIRED}/V_{REF})(65536)$
$Z5 = (1.5/5)(65536) = 19660.8$
$0 \leq Zx \leq 65535$
$0.1V \leq \text{Zero DAC Analog Range} \leq (V_{SA} - 0.1V)$
$0V \leq \text{Zero DAC Programming Range} \leq V_{REF}$

For positive slopes (for example, ZM4):

$ZM4 = [(Z4 - Z3)/(T4 - T3)][256]$
$ZM4 = [(26214.4 - 13107.2)/(0 - \{-160\})][256] = 20971.52$
Integer [20971.52] = 20972
ZM4 = 20972 → 51ECh → 0101 0001 1110 1101

For negative slopes (for example, ZM6):

$ZM6 = [(Z6 - Z5)/(T6 - T5)][256]$
$ZM6 = [(13107.2 - 19660.8)/(320 - 160)][256] = -10485.76$
Integer [−10485.76] = −10486
Generate the Twos Complement of −10486:
ZM6 = D70Ah → 1101 0111 0000 1010

NOTE: Zero DAC Slopes

If the Zero DAC slope computes to a count > 65535, there is a problem. The Temp ADC must be reconfigured for lower resolution or the number of points in the Lookup Table must be increased to bring the slopes within the PGA309 computation region.

Table 3-4. Zero DAC Temperature Coefficient Calculation

Temp (°C)	Temp Index	Temp ADC (Counts)	Zero DAC Desired Value	Zero DAC Desired Index	Zero DAC Desired (Counts)	Zero DAC Slope	Zero DAC Slope Formula	Zero DAC Slope (1) (Counts)	Zero DAC Slope (Hex)
−40	T0	−640	0.1	Z0	1310.7	Z0	Z0 = Z0	1311	051F
−30	T1	−480	0.2	Z1	2621.4	ZM1	ZM1 = [(Z1 − Z0)/T1 − T0)][256]	2097	0831
−20	T2	−320	1	Z2	13107.2	ZM2	ZM2 = [(Z2 − Z1)/T2 − T1)][256]	16777	4189
−10	T3	−160	1	Z3	13107.2	ZM3	ZM3 = [(Z3 − Z2)/T3 − T2)][256]	0	0000
0	T4	0	2	Z4	26214.4	ZM4	ZM4 = [(Z4 − Z3)/T4 − T3)][256]	20972	51EC
10	T5	160	1.5	Z5	19660.8	ZM5	ZM5 = [(Z5 − Z4)/T5 − T4)][256]	−10486	D70A
20	T6	320	1	Z6	13107.2	ZM6	ZM6 = [(Z6 − Z5)/T6 − T5)][256]	−10486	D70A
30	T7	480	2	Z7	26214.4	ZM7	ZM7 = [(Z7 − Z6)/T7 − T6)][256]	20972	51EC

(1) Integer [Zero DAC Slope Formula].

Step 4:

Assemble the Lookup Table, as shown in Table 3-5.

Table 3-5. Lookup Table Contents

Temp (°C)	Temp Index	Zero DAC Slope	Gain DAC Slope	EEPROM Tx (Hex)	EEPROM ZMi (Hex)	EEPROM GMi (Hex)
−40	T0	Z0	G0	FD80	051F	FFFF
−30	T1	ZM1	GM1	FE20	0831	C291
−20	T2	ZM2	GM2	FEC0	4189	851F
−10	T3	ZM3	GM3	FF60	0000	4800
0	T4	ZM4	GM4	0000	51EC	D700
10	T5	ZM5	GM5	00A0	D70A	A3D7
20	T6	ZM6	GM6	0140	D70A	B392
30	T7	ZM7	GM7	01E0	51EC	6DCB
—	T_{END}	ZM_{END}	GM_{END}	7FFF	0000	B5D8

Use the calculated values from Step 2 and Step 3.

Set TM_{END} to 7FFFh to indicate the end of the Lookup Table.

Set ZM_{END} to 0000h.

Calculate GM_{END} as Checksum2 (truncate results above 16-bit):

GM_{END} = Checksum2 = FFFFh − sum(Hex values of all entries in the Lookup Table except GM_{END})
GM_{END} = FFFFh − C4A27h
GM_{END} = FFFFF4B5D8h
GM_{END} = Checksum2 = B5D8h

Step 5:

Calculate Ideal value for Gain DAC at T_{READ} = +25°C using Table 3-6.

Table 3-6. Gain DAC vs Temperature

Tx	Temp (°C)	Gx	Gain DAC
T0	−40	G0	1
T1	−30	G1	0.9
T2	−20	G2	0.7
T3	−10	G3	0.4
T4	0	G4	0.3333
T5	10	G5	0.6
T6	20	G6	0.4756
T_{READ}	25	G_{READ}	Calculated
T7	30	G7	0.6543

Linear Interpolation for Gain DAC (T_{READ} = 25°C):

$G_{READ} = \{[(G7 - G6)/(T7 - T6)]\ [T_{READ} - T6]\} + G6$
$G_{READ} = \{[(0.6543 - 0.4756)/(30 - 20)]\ [25 - 20]\} + 0.4756$
$G_{READ} = 0.56495$

Step 6:

Reference calculation algorithm for Gain DAC using Lookup Table.

Table 3-7 outlines the calculation algorithm used inside the PGA309 for linear interpolation and calculation of the Gain DAC setting for T_{READ} = 25°C. From Table 3-3 the computations for GM1-GM7 at T1-T7, for given values at G1-G7, are known. In addition, the starting values (T0 and G0) were defined. Step 5 shows the Actual Gain DAC value for T_{READ} = 25°C should be 0.56495 V/V if the linear interpolation part of the calculation algorithm is working properly.

Table 3-7. Gain DAC Lookup Table Calculation Algorithm

Temp (°C)	Tx	Temp ADC (Counts)	GMi	Gain DAC Slope (1) (Counts)	GAC Calculation	Running GAC Value (1) (Counts)	Actual Gain DAC (V/V)
−40	T0	−640	G0	65535	GAC0 = G0	65535	0.9999898
−30	T1	−480	GM1	−15727	GAC1 = GAC0 + [GM1(T1 − T0)/256]	55706	0.9000041
−20	T2	−320	GM2	−31457	GAC2 = GAC1 + [GM2(T2 − T1)/256]	36045	0.7000020
−10	T3	−160	GM3	−47104	GAC3 = GAC2 + [GM3(T3 − T2)/256]	6605	0.4005229
0	T4	0	GM4	−10496	GAC4 = GAC3 + [GM4(T4 − T3)/256]	45	0.3337911
10	T5	160	GM5	41943	GAC5 = GAC4 + [GM5(T5 − T4)/256]	26259	0.6004537
20	T6	320	GM6	−19566	GAC6 = GAC5 + [GM6(T6 − T5)/256]	14030	0.4760539
30	T7	480	GM7	28107	T7 > T_{READ} → YES!	—	—
25	T_{READ}	400	—	—	GAC_TREAD = GAC6 + [GM7(T_{READ} − T6)/256]	22813	0.565399169
—	T_{END}	32767 (7FFFh)	—	—	The Lookup Table is read to the end to verify Checksum2	—	—

(1) Integer [GAC Calculation].

Each time the Temp ADC does a conversion, it reads the entire external EEPROM. The first part of the EEPROM is dedicated to fixed setup parameters for the PGA309 that do not change with temperature. As the PGA309 reads the second half of the EEPROM, it begins a running calculation of the Gain DAC setting with temperature (the PGA309 runs a similar calculation for the Zero DAC setting). The model in Table 3-7 includes an accumulator named GAC (G Accumulator). When the PGA309 reads T0, the initial Gain DAC setting (G0) is stored in GAC0 (GAC at T0READ). Next, T1 is read and slope GM1 is multiplied by the difference between T1 and T0 (a scale divisor of 256 is used to convert back to decimal counts for our model) and added to GAC0 to form the new accumulator value, GAC1 (GAC at T1READ). This process continues in a sequential fashion as the PGA309 reads through the entire Lookup Table. As each temperature index value (Tx) is read, it is compared against T_{READ}, the current Temp ADC conversion result. If Tx > T_{READ}, it is known that T_{READ} is between Tx and T(x − 1). In this example, it occurs after T7 is read. The accumulator contents, GAC6 (GAC at T6), are modified by the addition of (T_{READ} − T6)(GM7).

The resulting GAC_TREAD is the linearly interpolated setting for the Gain DAC at T_{READ} = 25°C. The actual Gain DAC value is slightly different than the theoretical value calculated in Step 5 due to Gain DAC resolution and computation rounding. The rest of the EEPROM is read through T_{END} for error checking with Checksum2 at the end of the Lookup Table. If Checksum2 is valid then the Gain DAC is updated with the computed value GAC_TREAD = 0.565399169.

GAC Calculation (for example, GAC2):

GAC1 = 55706; GM2 = −31457; T2 = −320; T1 = −480
GAC2 = GAC1 + [GM2(T2 − T1)/256]
GAC2 = 55706 + [−31457(−320−{−480})/256] = 36045.375
Integer [GAC2] = Integer [36045.375] = 36045
GAC2 = 36045

Actual Gain DAC (for example, GAC2):

GAC2 = 36045
Gain DAC = [(GACx/65536)(2/3)] + 1/3
Gain DAC = [(36045 / 65536)(2/3)] + 1/3 = 0.7000020
Gain DAC at GAC2 = 0.7000020

3.3 Checksum Error Event

If at any time the PGA309 detects an invalid Checksum1 from the first part of the EEPROM, the PGA309 will disable V_{OUT}, wait for approximately 33ms, and try to read the EEPROM again from the beginning. It will continue to reread the EEPROM indefinitely.

If at any time the PGA309 detects an invalid Checksum2 from the second part of the EEPROM (the Lookup Table data), it will disable V_{OUT}, set the Gain and Zero DACs to their POR values, return to the read configuration register portion (first part of the EEPROM) of the loop, and then try to read the EEPROM Lookup Table again when the next temperature conversion completes.

3.4 Test Pin

The PGA309 has a user-accessible test pin (Test, pin 9), which stops the internal state machine cycle and enables the output drive (V_{OUT}) when it is brought high (logic ‘1’). This mode can be used for ease of troubleshooting or initial configuration diagnostics during the system design. During normal (stand-alone) operation, the Test pin must be connected to GND (logic ‘0’).

If the Test pin is brought high at any time, the following happens:

- The state machine described previously is interrupted and reset to its initial state. Any EEPROM transactions are interrupted and the Two-Wire bus is released.
- The PGA309 output (V_{OUT}) is enabled.
- All internal registers are kept to their current values. If the Test pin is high when the supply becomes valid, the registers stay in the initial (POR) state and output is enabled immediately.
- An external controller can modify any of the writable PGA309 registers using either a One-Wire or Two-Wire digital interface.

In this mode, a test signal can be applied to the front end of the PGA309, which quickly verifies if the signal path through the PGA309 is functioning correctly.

Test mode (Test pin = high) is recommended during initial calibration because the values in the external EEPROM are ignored and the PGA309 registers can be individually set as desired.

3.5 Power-On Initial Register States

In a power-up or low-voltage event, the POR circuit resets all the PGA309 registers to their initial state. All registers are set to zeros except for the Gain and Zero DACs, which both are set to 4000h.

Table 3-8 summarizes the key settings for the POR states.

Table 3-8. POR States for Key Parameters

Parameter	POR State
Coarse Offset	0V
Front-End PGA Gain	4 ($V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$)
Gain DAC	0.5
Output Amplifier Gain	2
Zero DAC	$0.25V_{REF}$
V_{REF} Select	External Reference
Lin DAC	0
Fault Monitor	Disabled
Over/Under-Scale	Disabled
V_{EXC}	Disabled
I_{TEMP}	Disabled
Temp ADC	External Signal Mode

Example 3-2 and Figure 3-5 show by example how the PGA309 functions on power-up with the Test pin high.

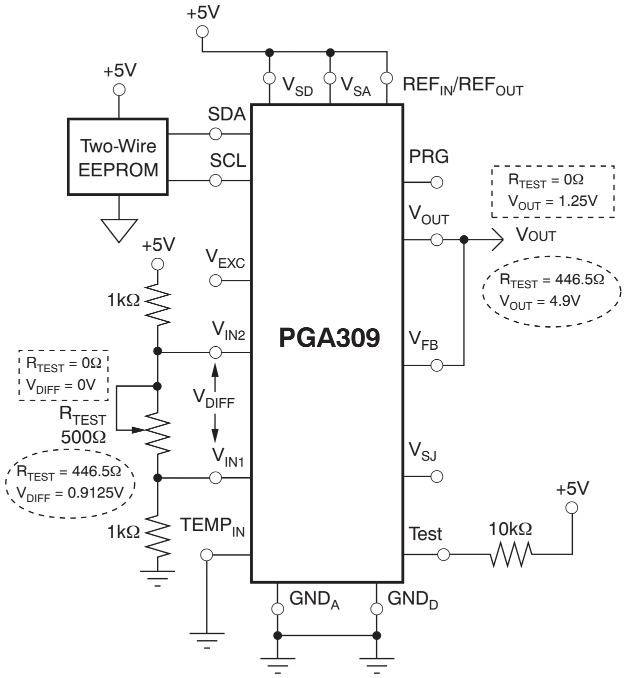
Example 3-2. PGA309 Power-Up State

For a +5V supply and configuration as shown in Figure 3-5 with Test pin high, the gain and offset scaling through the PGA309 on power-up becomes:

$V_{OUT} = V_{DIFF}$ (Front-End PGA Gain)(Output Amplifier Gain)(Fine Gain) + $0.25V_{REF}$(Fine Gain)(Output Amplifier Gain)

$V_{OUT} = V_{DIFF}(4)(2)(0.5) + (0.25(5)(0.5)) \times 2$

$V_{OUT} = 4\,V_{DIFF} + 1.25V$



NOTE: Two conditions for V_{DIFF} and the resulting V_{OUT} are shown in this figure. Condition one is in a dashed, square box. Condition two is shown in a dashed oval.

Figure 3-5. Signal Path Functional Check with Test = ‘1’ on Power-Up

Chapter 4

SBOU024B–August 2004–Revised January 2011

Digital Interface

This chapter describes the digital interface of the PGA309.

Topic **Page**

4.1 Description

There are two digital interfaces on the PGA309. The PRG pin uses a One-Wire, UART-compatible interface, with bit rates from 4.8kbits/s (4800 baud) to 38.4kbits/s (38400 baud). The SDA and SCL pins together form an industry standard Two-Wire interface at clock rates from 1kHz to 400kHz. The external EEPROM uses the Two-Wire interface for programming and reading. Communication to the PGA309 internal registers can be conducted through either digital interface, One-Wire or Two-Wire. Additionally, the external EEPROM can be programmed either through the PGA309 One-Wire interface pin, PRG, or by direct connection to the SDA and SCL lines of the Two-Wire interface.

4.2 Two-Wire Interface

The industry standard Two-Wire timing diagram is shown in Figure 4-1, with the timing diagram definitions in Table 4-1. The key operating states are:

- Bus Idle: Both SDA and SCL lines remain high.
- START Condition: A START condition is defined by a change from high to low in the state of the SDA line, while the SCL line is high. Each data transfer is initiated with a START condition (see Figure 4-1).
- STOP Condition: A STOP condition is defined by a change from low to high in the state of the SDA line, while the SCL line is high. Each data transfer is terminated with a repeated START or STOP condition (see Figure 4-1).
- Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of each 8-bit byte of data.
- Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device acknowledges by pulling down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the master may terminate the transaction by generating a Not Acknowledge on the last byte that has been transmitted by the slave (see Figure 4-2).

Table 4-1. Two-Wire Timing Diagram Definitions

Parameter		Min	Max	Units
SCL Operating Frequency	f_{SCL}	1	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}	600		ns
Hold Time After Repeated START Condition. After this period, the first clock is generated.	t_{HDSTA}	600		ns
Repeated START Condition Setup Time	t_{SUSTA}	600		ns
STOP Condition Setup Time	t_{SUSTO}	600		ns
Data Hold Time	t_{HDDAT}	0		ns
Data Setup Time	t_{SUDAT}	100		ns
SCL Clock LOW Period	t_{LOW}	1300		ns
SCL Clock HIGH Period	t_{HIGH}	600		ns
Clock/Data Fall Time	t_F		300	ns
Clock/Data Rise Time	t_R		300	ns

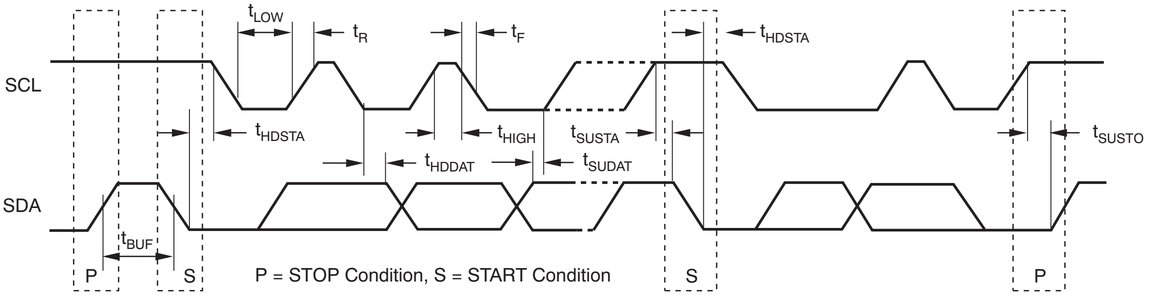


Figure 4-1. Two-Wire Timing Diagram

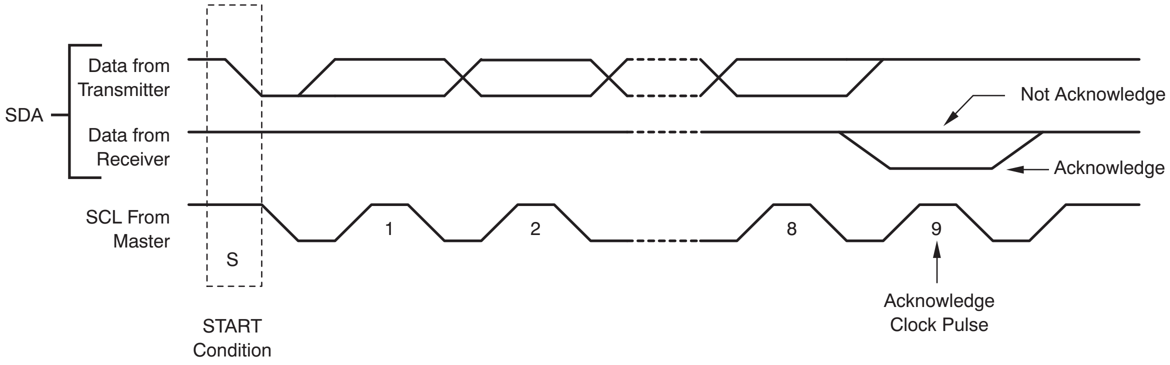


Figure 4-2. Two-Wire Start and Acknowledge

4.2.1 Device Addressing

Following a START condition issued by the master, a control byte is the first byte received. The seven most significant bits (MSBs) of the control byte are the slave address for the part being addressed. The last bit of the control byte is a Read/Write control bit (Read = ‘1’, Write = ‘0’). The slave addresses for the PGA309 and supported external EEPROM are shown in Figure 4-3.

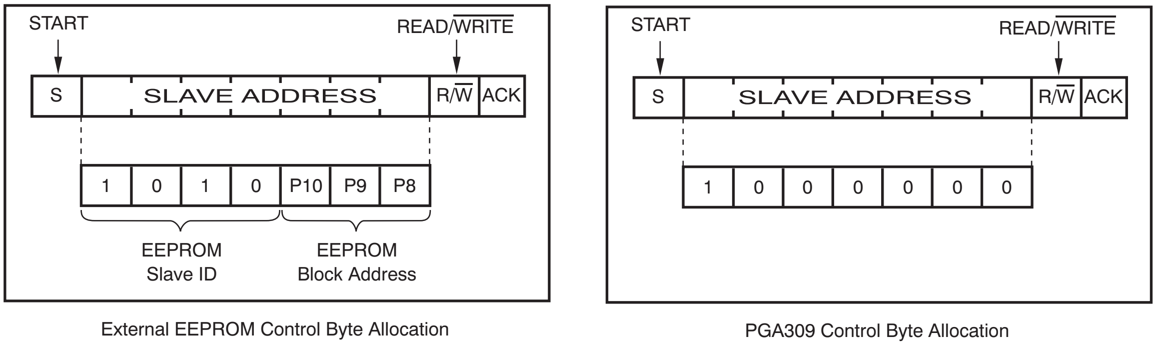
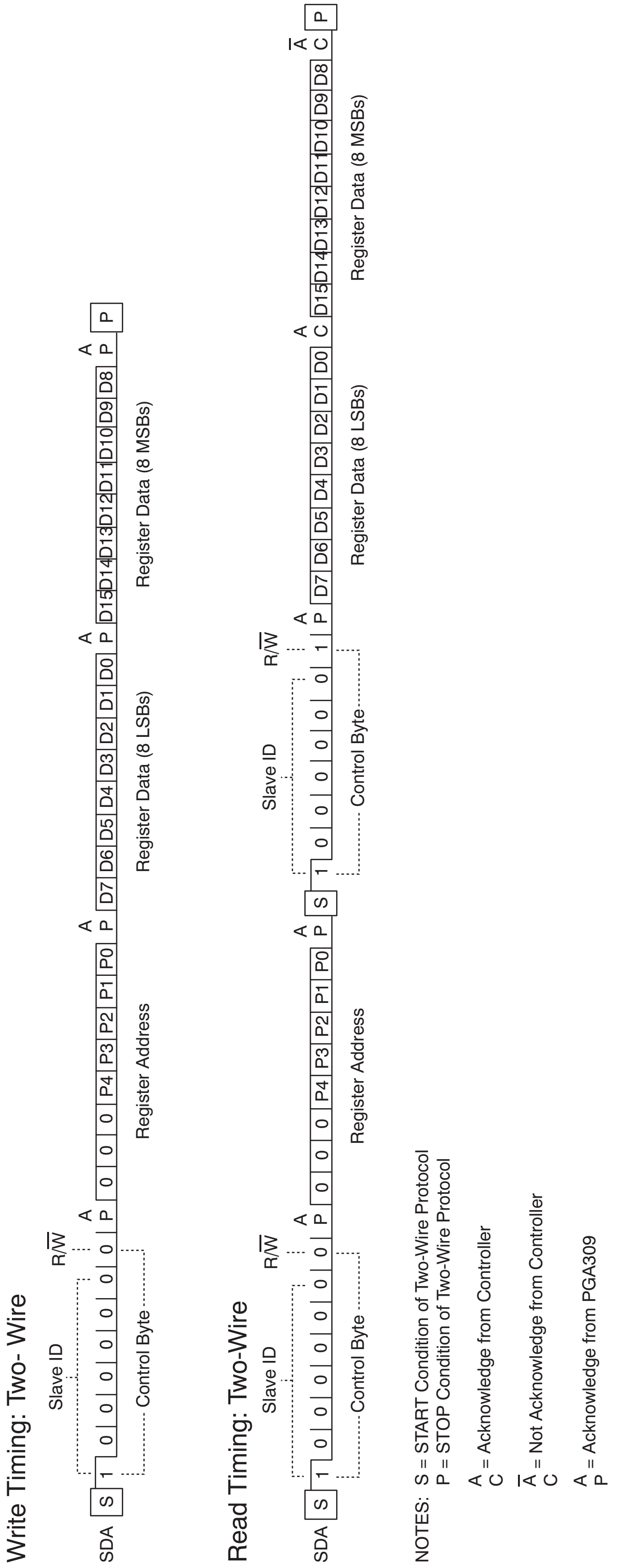


Figure 4-3. External EEPROM and Control Byte Allocation

4.2.2 Two-Wire Access to PGA309

Figure 4-4 shows the Two-Wire read and write timing supported for interfacing directly with the PGA309 internal registers.



NOTES: S = START Condition of Two-Wire Protocol
P = STOP Condition of Two-Wire Protocol

A
C = Acknowledge from Controller

$\overline{A}$
C = Not Acknowledge from Controller

A
P = Acknowledge from PGA309

Figure 4-4. Two-Wire Access to PGA309 Timing

4.3 One-Wire Interface

The PGA309 may be configured through a One-Wire UART-compatible interface (PRG pin). This interface also allows programming of the external industry-standard Two-Wire EEPROM device. There are six possible communication transactions. These transactions allow the internal register pointer to be updated, the external EEPROM pointer to be updated, internal registers to be read, internal registers to be written, EEPROM data to be read, and EEPROM data to be written. It is possible to connect the PRG pin, which uses the One-Wire interface, to the V_{OUT} pin in true three-wire sensor module applications and still allow for digital programming.

Each transaction consists of several bytes of data transfer. Each byte consists of 10 bit periods. The first bit is the start bit and is always zero. The PRG pin should always be high when no communication is in progress. The one-to-zero (high-to-low) transition of the PRG pin signals the start of a byte transfer and all timing information for the current byte is referenced to this transition. Bits 2 thru 9 are the eight data bits for the byte and are transferred least significant bit (LSB) first. The tenth bit is the stop bit and is always ‘1’. The recommended circuit implementation to interace to the PRG pin uses a pull-up resistor and/or pull-up current source with an open drain (or open collector) driver connected to the PRG pin. (The PRG pin is also an open drain output. The PRG pin may be driven high by the digital programmer (controller) during transmit from the controller, but some form of pull-up will be required to allow the signal to go high during a receive transaction, since the PGA309 can only pull the output low. Figure 4-5 shows a typical connection between the PGA309 PRG pin and the controller.

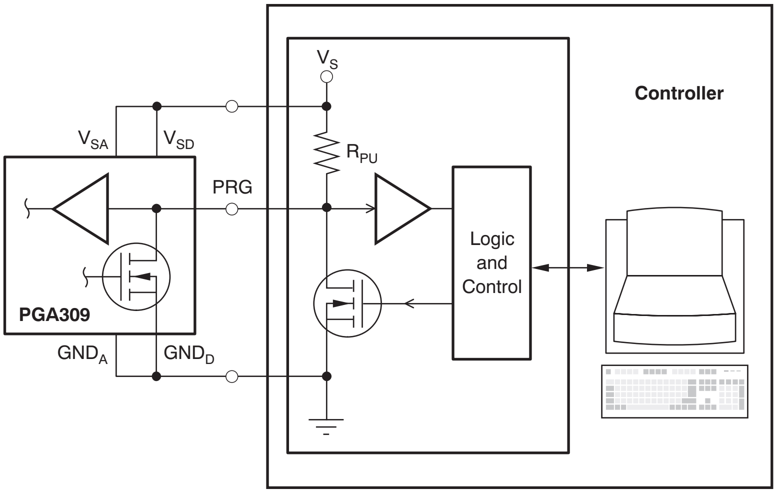


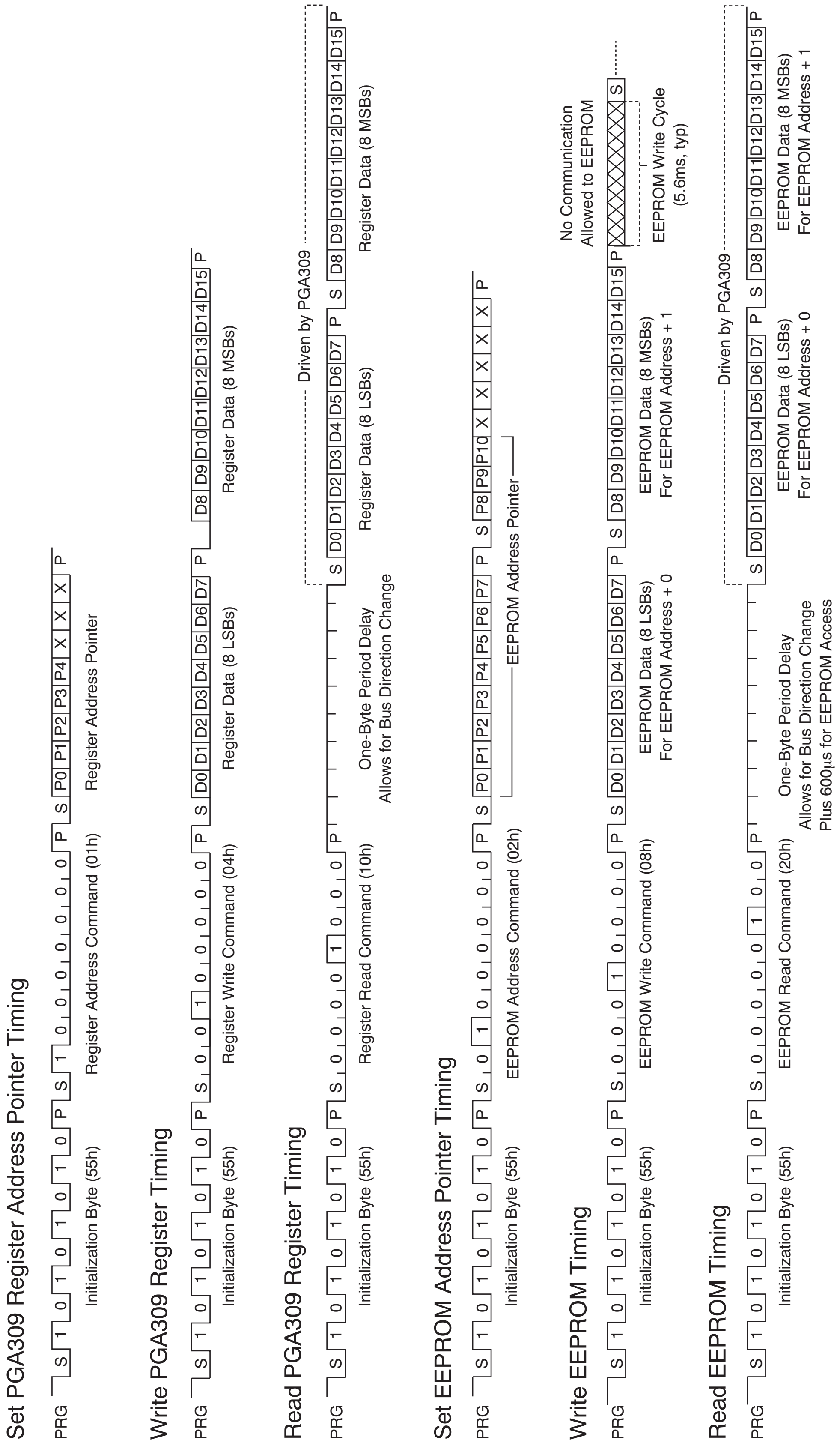
Figure 4-5. Typical PGA309 PRG To Controller Connection

All communication transactions start with an initialization byte transmitted by the controller. This byte (55h) is used to sense the baud rate used for the communication transaction. The baud rate is sensed during the initialization byte of every transaction. This baud rate is used for the entire transaction. Each transaction may use a different baud rate if desired. Baud rates of 4800 to 38400 are supported. The second byte is a command byte transmitted by the controller.

There are six possible commands:

- Set PGA309 Register Address Pointer (01h)
- Set EEPROM Address Pointer (02h)
- Write PGA309 Register (04h)
- Write EEPROM (08h)
- Read PGA309 Register (10h)
- Read EEPROM (20h)

See Figure 4-6 for timing details of these transactions.



NOTES: S = START Condition of One- Wire Protocol
P = STOP Condition of One- Wire Protocol
Unless otherwise noted, all transactions are driven by the controller.

Figure 4-6. One-Wire (PRG) Access to PGA309 and External EEPROM Timing

Data transfer occurs after the command byte. The number of bytes and direction of data transfer depend on the command byte.

For the Set PGA309 Register Address Pointer (01h) command, one additional byte is required to be transmitted by the controller. This is used to select the PGA309 internal register for the next PGA309 Write Register (04h) or PGA309 Read Register (10h) command. For the PGA309 Write Register command, two additional bytes are required to be transmitted by the controller. These two bytes, transmitted least significant byte first, are stored in the PGA309 internal register pointed to by the register address pointer. The addressed register will be updated with all 16 bits simultaneously at the completion of the transfer of the second byte. For the PGA309 Read Register (10h) command, two additional bytes are transmitted by the PGA309. The PGA309 waits for eight bit periods after the completion of the command byte before beginning transmission. This allows time for the controller to ensure that the PGA309 will be able to control the One-Wire interface. The first byte transmitted is the least significant byte of the register and the second byte is the most significant byte of the register.

For a One-Wire PGA309 sequence, the transactions may be repeated immediately one after the other, as shown in Figure 4-7. For a One-Wire PGA309 register read sequence, the transactions may be repeated after the data has been received from the PGA309, also shown in Figure 4-7.

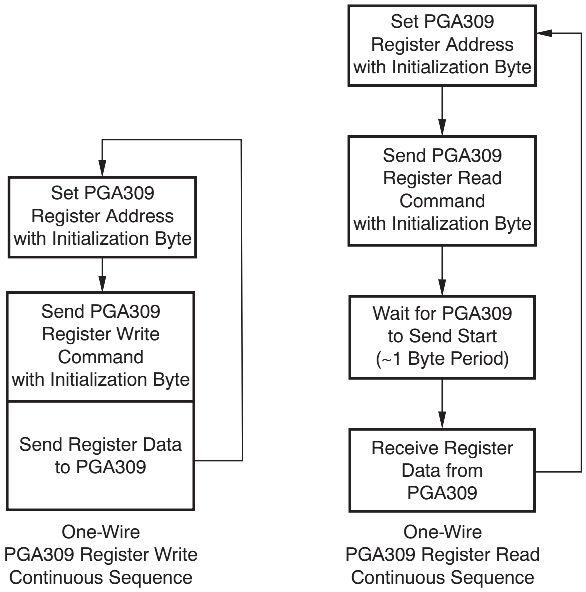


Figure 4-7. One-Wire Access to PGA309 Registers

For the Set EEPROM Address Pointer (02h) command, two additional bytes must be transmitted by the controller. These are used for the EEPROM address for the next Write EEPROM (08h) or Read EEPROM (20h) command. For the Write EEPROM (08h) command, two additional bytes are transmitted by the controller. These two bytes are written to the EEPROM and stored at the address contained in the EEPROM address pointer. The first byte (least significant byte) is written to the address in the EEPROM address pointer. The second byte (most significant byte) is written to the address in the EEPROM address pointer plus one. To avoid any confusion, the EEPROM address pointer is always set to a value that is even. The first byte is written to the even address and the second byte is written to the next consecutive odd address.

The controller is responsible for ensuring that the EEPROM device has enough time to successfully complete the write operation before additional EEPROM communication occurs. For a typical EEPROM, this will be about 5.6ms (0.6ms for the PGA309 to write a 16-bit byte into the EEPROM and 5ms for the EEPROM nonvolatile internal write cycle). For the Read EEPROM (20h) command, two additional bytes are transmitted by the PGA309. The PGA309 waits for eight bit periods after the completion of the command byte to allow time for data direction change. The PGA309 also waits for a read communication from the EEPROM device to occur. This will typically be 600μs of additional delay. The first byte transmitted is the least significant byte (from EEPROM address) and the second byte transmitted is the most significant byte (from EEPROM address + 1).

For continuous One-Wire PGA309 EEPROM writes, the controller must insert a typical 5.6ms delay between transactions, as shown in Figure 4-8. For continuous One-Wire PGA309 EEPROM reads, transactions may be repeated after the data has been received from the PGA309, as shown in Figure 4-8.

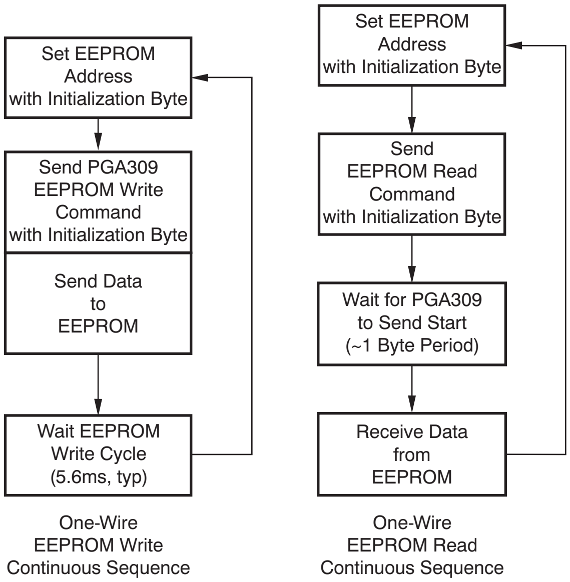


Figure 4-8. One-Wire Access to External EEPROM

If there is an invalid communication transaction or disconnect with the EEPROM, a One-Wire EEPROM Read will be all 1s.

4.4 One-Wire Interface Timeout

A timeout mechanism is implemented to allow for resynchronization of the One-Wire interface, or if synchronization between the controller and the PGA309 is lost for any reason. The timeout period is set to approximately 25ms to 35ms. If the timeout period expires between the initialization byte and the command byte, between the command byte and any data byte, or between any data bytes, the PGA309 will reset the One-Wire interface circuitry to expect an initialization byte. Every time a byte is transmitted on the One-Wire interface, this timeout period is restarted.

4.5 One-Wire Interface Timing Considerations

Figure 4-9 illustrates the key timing and jitter considerations for the One-Wire interface and Table 4-2 contains the specifications for ensured, reliable operation. During a transaction, the baud rate must remain within ±1% of its initialization byte value; however, the baud rate can change from transaction to transaction.

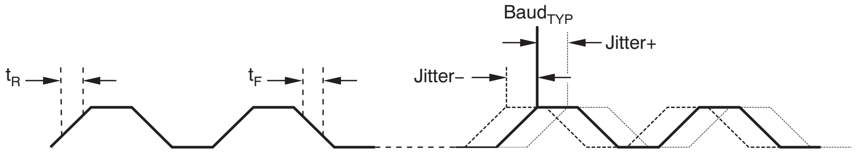


Figure 4-9. One-Wire Through PGA309 Timing Diagram

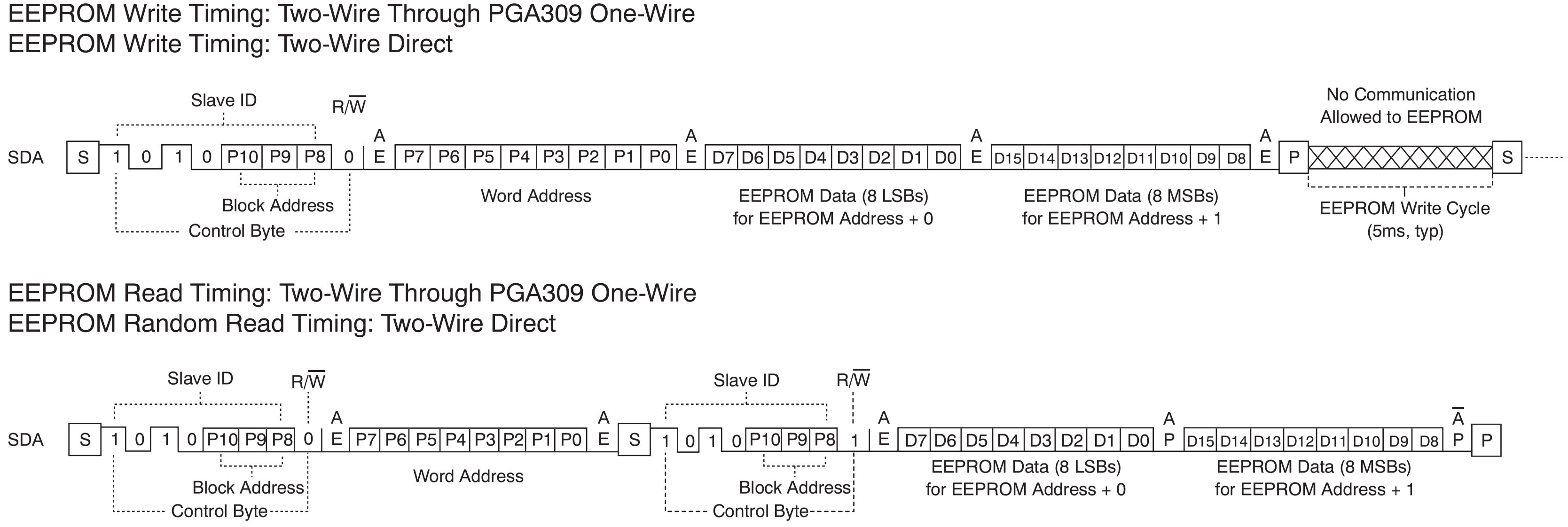
Table 4-2. One-Wire Timing Diagram Definitions

Parameter	Min	Typ	Max	Units
Baud	4.8K		38.4K	Bits/s
Rise Time, t_R			0.5	%Baud
Fall Time, t_F			0.5	%Baud
Jitter (1)			±1	%Baud

(1) Transmit jitter from controller to PGA309. Standard UART interfaces will accept data sent from the PGA309 during One-Wire transactions.

4.6 Two-Wire Access to External EEPROM

Figure 4-10 shows the read and write timing for the PGA309 interface to the external EEPROM when the PGA309 receives commands through the One-Wire interface (PRG pin). All manufacturer reading and writing modes are allowed when direct Two-Wire access is made to the external EEPROM. Note that full 10-bit EEPROM addressing mode is supported by the PGA309 One-Wire access to the external EEPROM through the PGA309 Two-Wire interface. A 1k-bit EEPROM minimum is needed for the PGA309 Configuration Register and 17 Lookup Table coefficients. A larger EEPROM can be used to store other configuration information such as serial number, date code, lot code, etc. In addition, note that the PGA309 SCL and SDA pins have light internal pull-up current sources to V_{SD} (85μA typical on each pin). This is more than adequate for most applications that involve placing only the external EEPROM close to the PGA309 on the same printed circuit board (PCB). Other applications that add load and capacitance to the SDA and SCL lines may need additional external pull-up resistors to V_{SD} to ensure rise timing requirements are met at all times. At the end of a EEPROM write cycle, there is a typical 5ms EEPROM write cycle during which the data is stored in a nonvolatile fashion internally to the EEPROM. During this time, if Two-Wire direct access is attempted, there will be no acknowledge from the EEPROM. If communicating to the external EEPROM through the PGA309 One-Wire interface, this EEPROM write cycle time is a No Communication Allowed time period.



NOTES: S = START Condition of Two-Wire Protocol
P = STOP Condition of Two-Wire Protocol

$\substack{A\\P}$ = Acknowledge from PGA309

$\substack{\overline{A}\\P}$ = Not Acknowledge from PGA309

$\substack{A\\E}$ = Acknowledge from EEPROM

Figure 4-10. Two-Wire Access to External EEPROM Timing

4.7 One-Wire Interface Initiated Two-Wire EEPROM Transactions

The Write EEPROM and Read EEPROM One-Wire commands initiate a communication transaction on the Two-Wire bus between the PGA309 and the EEPROM device (see Figure 4-10).

The Write EEPROM command causes the PGA309 to generate a Two-Wire start condition and send a Two-Wire slave address byte to the EEPROM device with the four MSBs set to ‘1010’ and the three LSBs set to bits 10−8 of the EEPROM address pointer. The $R/\overline{W}$ bit is set to ‘0’ to indicate a write instruction. If the PGA309 receives an acknowledge from the EEPROM device, it then sends a byte with eight LSBs of the EEPROM address pointer. If the PGA309 receives an acknowledge from this byte, the PGA309 sends the least significant byte of the data to the EEPROM. Upon successful receipt of an acknowledge to this byte, the PGA309 transmits the most significant byte. After the acknowledge bit of this byte, the PGA309 generates a Two-Wire stop condition to terminate data transfer to the EEPROM.

The Read EEPROM command causes the PGA309 to generate a Two-Wire start condition and send a Two-Wire slave address byte to the EEPROM with the four MSBs set to ‘1010’, the three LSBs set to bits 10−8 of the EEPROM Address Pointer, and the R/W bit set to ‘0’ to indicate a write instruction. If the PGA309 receives an acknowledge from the EEPROM device, it will then send a byte with the eight LSBs of the EEPROM address pointer. If the PGA309 receives an acknowledge from this byte, the PGA309 generates another Two-Wire START condition, send another slave address byte but this time with the $R/\overline{W}$ bit set to ‘1’ to indicate a read instruction. If the PGA309 receives an acknowledge, it continues to clock the SCL line to receive the first byte from the EEPROM, acknowledge this byte, receive the second byte, not acknowledge the second byte to terminate data transfer, and then generate a Two-Wire STOP condition.

4.8 PGA309 Stand-Alone Mode and Two-Wire Transactions

In Stand-Alone Mode (see Chapter 3, Operating Modes), the PGA309 accesses the external EEPROM in a different fashion than that presented for the One-Wire Interface Initiated Two-Wire Transactions. If all other POR conditions have been met to allow a PGA309 to allow access to a properly programmed external EEPROM, the PGA309 will first access the first part of the external EEPROM (configuration register data) as shown in Figure 4-11.

If the Checksum1 is correct and the PGA309 is triggered by the Temp ADC to read the second part of the EEPROM, it will proceed as shown in Figure 4-12. If the One-Wire disable bit, OWD, bit 15, in Register 4 is set to ‘1’, initial POR is completed, and a valid Checksum2 is received, the One-Wire interface will be disabled, the PRG pin becomes high impedance, and One-Wire communication cannot take place unless power is cycled. This is necessary to allow for direct connection of the PRG pin to V_{OUT}.

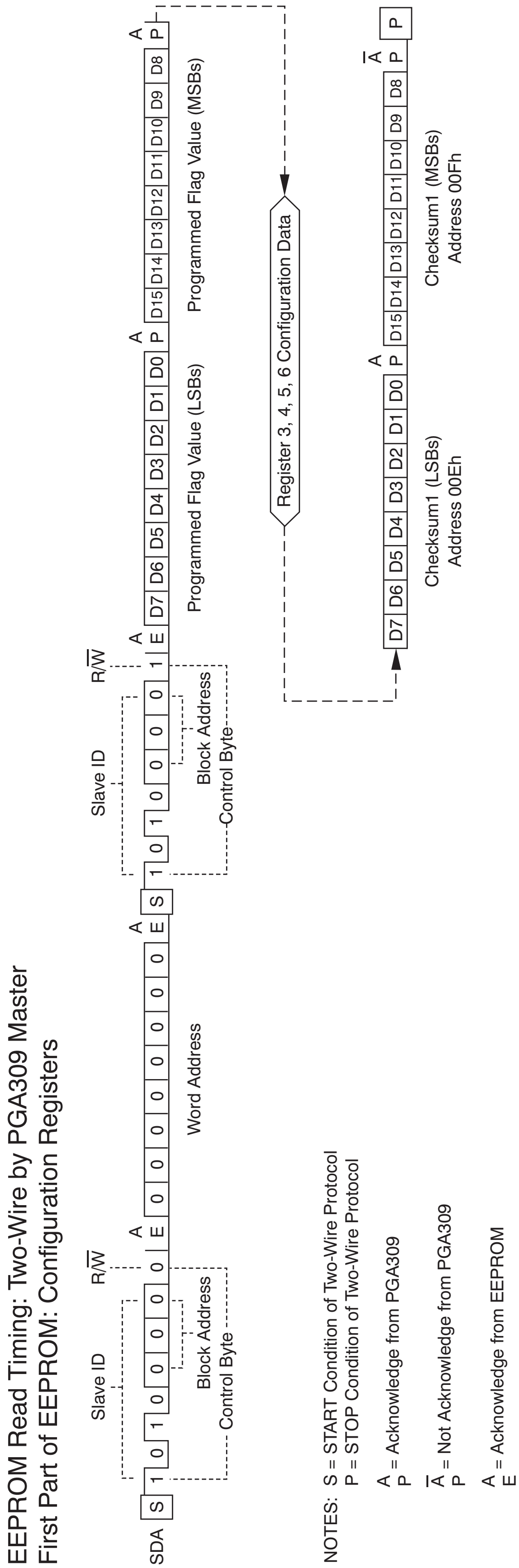


Figure 4-11. First Part of External EEPROM Timing for Stand-Alone Mode

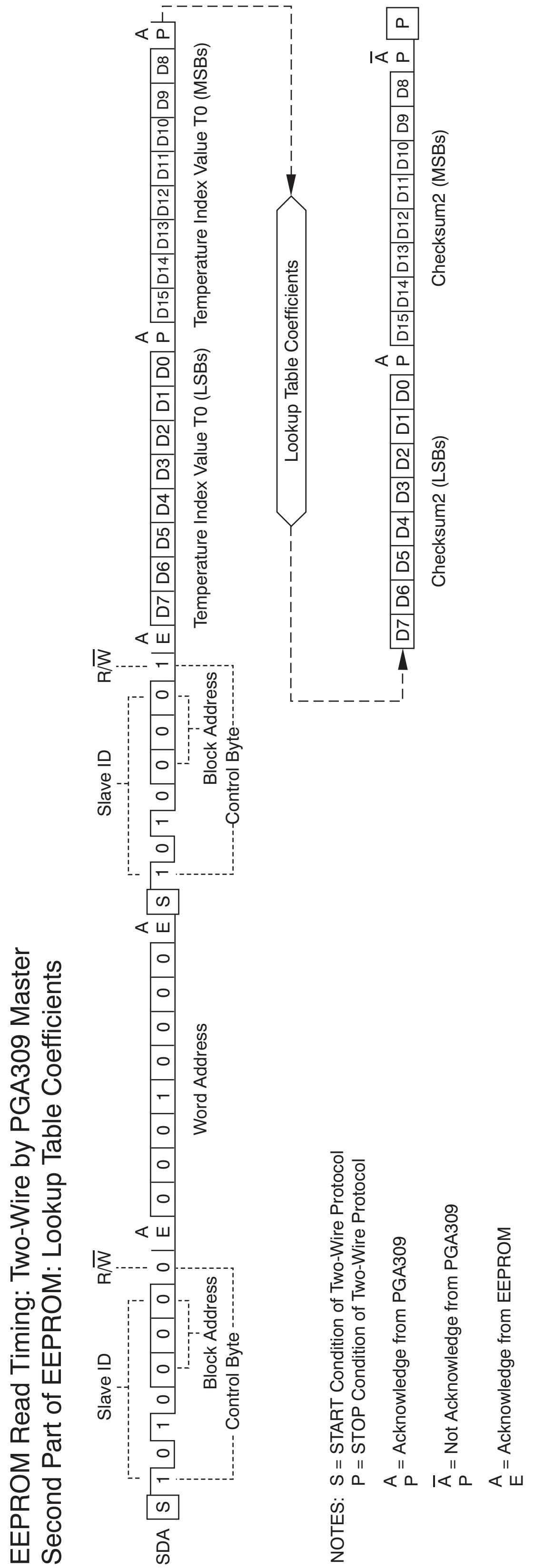


Figure 4-12. Second Part of External EEPROM Timing for Stand-Alone Mode

4.9 PGA309 Two-Wire Bus Master Operation and Bus Sharing Considerations

Whenever the PGA309 is called upon to communicate to the external EEPROM, the PGA309 must become the master on the Two-Wire interface bus. In order to do this in a reliable and orderly fashion, the PGA309 contains fault diagnostics to attempt to free a stuck bus. Several monitors and algorithms check for bus availability, prevent bus contention in case other devices are connected in parallel with the External EEPROM.

If the PGA309 is ever addressed on its Two-Wire or One-Wire interface, with the PGA309 providing a successful acknowledge, the PGA309 will cease all transactions as a master on the Two-Wire bus and give up control for 1.3 seconds. Each time the PGA309 is addressed on the Two-Wire bus, the 1.3 second timeout is reset, as shown in Figure 4-13.

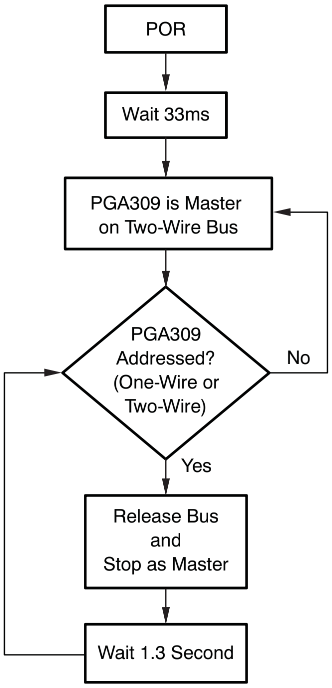


Figure 4-13. Two-Wire Bus Relinquish by PGA309 in Master Mode

Figure 4-14 details the algorithms used by the PGA309 when it must become master on the Two-Wire bus. A 33ms timer is started. Now SCL is monitored for being low. If SCL is not low, the PGA309 checks to see if communication on the Two-Wire bus is between a START and a STOP. If the bus communication is between a START and a STOP, the PGA309 waits for the 33ms timer to time out, and then checks if SDA is low. If SDA is not low and SCL is high, the PGA309 becomes bus master. If there is any SCL activity during the 33ms interval, the 33ms timer will restart.

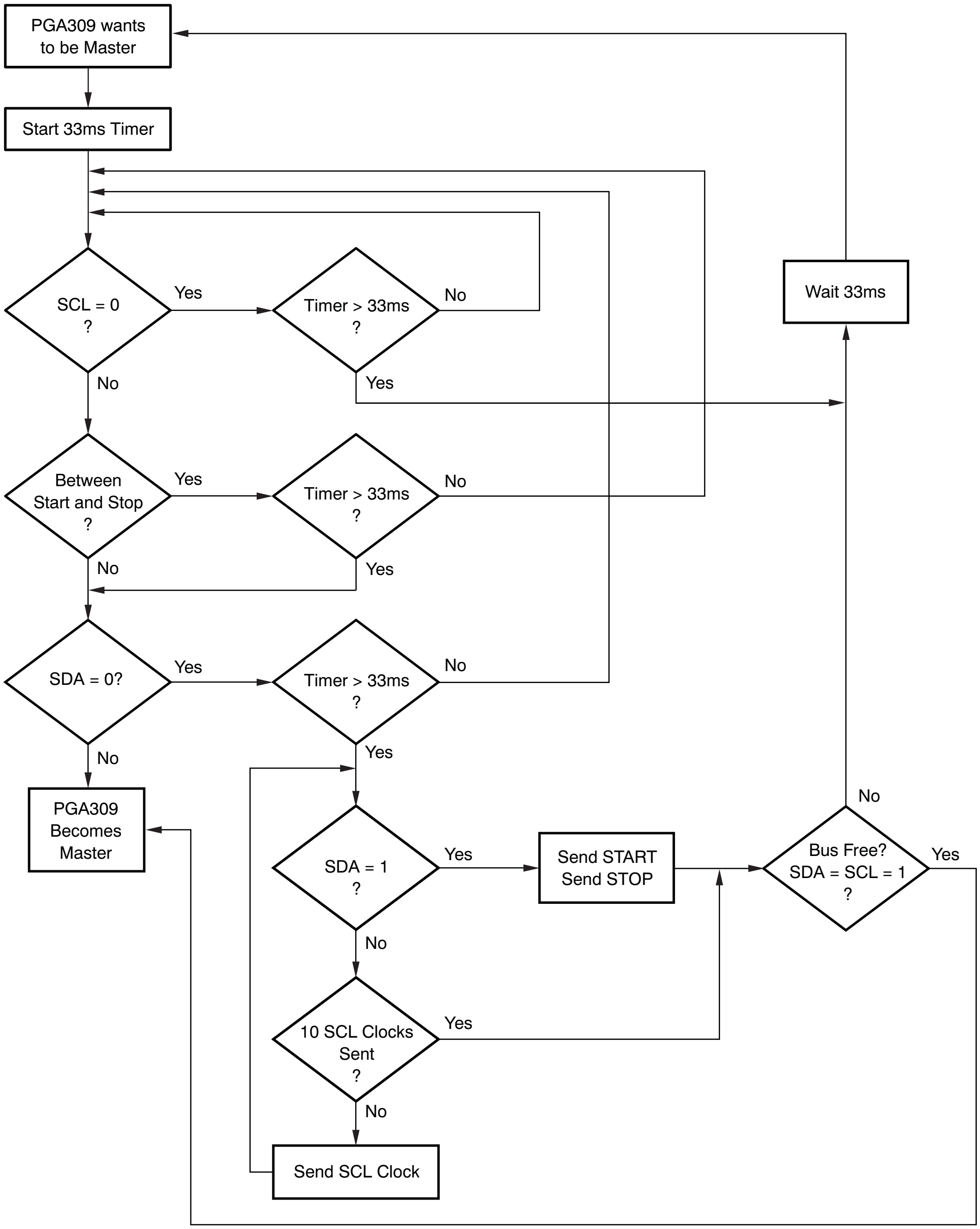


Figure 4-14. Two-Wire Bus Master Algorithm

If SCL remains low for the entire 33ms timer countdown, the PGA309 waits 33ms before starting the 33ms timer again to begin to check the bus for an idle state (SDA = SCL = ‘1’).

If SDA is low after the 33ms timer counts down, the PGA309 interprets this as a stuck-bus condition. The PGA309 attempts to free the stuck bus by sending up to ten clocks down SCL to free up SDA. If it is successful in causing SDA to go high, the PGA309 sends a START and then STOP sequence to ensure a complete reset of whichever device was causing the stuck bus. Now the bus should be in an idle state (SDA = SCL = ‘1’) and the PGA309 can become the master on the bus.

If the PGA309 is communicating on the bus as a master and it sees contention, the PGA309 will release the bus and retry in 33ms. Contention is defined as the PGA309 wanting SCL high and SCL is low, or wanting SDA high and SDA is low.

4.10 One-Wire Operation with PRG Connected to V_{OUT}

Some sensor applications, require the end-user access to three pins, V_S, GND, and Sensor Out. It is also desired in these applications to digitally calibrate the sensor module after its final assembly of sensor and electronics. The PGA309 has a mode that allows the One-Wire interface pin (PRG) to be tied directly to the PGA309 output pin (V_{OUT}), as shown in Figure 4-15.

For the PGA309 + sensor calibration, it is necessary to configure and reconfigure internal registers on the PGA309 and then measure the analog voltage on V_{OUT} as a result of these register value settings. To do this while V_{OUT} is tied to PRG requires the ability to enable and disable V_{OUT}. This allows a multiplexing operation between PRG using the connection as a bidirectional digital interface and V_{OUT} driving the connection as a conditioned sensor output voltage. In addition, it is convenient to configure the Temp ADC for Single Start Convert mode and delay the start of the Temp ADC until after V_{OUT} is enabled and internal circuitry has had a chance to settle to accurate final values. This is especially important in applications that use the Linearization Circuit, tie the sensor to V_{EXC}, and measure temperature external to the PGA309 (that is, a temperature sense series resistor in the upper or lower excitation leg of the bridge sensor).

Register 7 (Output Enable Counter Control Register) contains the control bits for setting both the amount of time V_{OUT} is active on the common connection and also the delay from the time V_{OUT} is enabled to the start of a Temp ADC conversion. These individual bits are defined in Table 4-3 and Table 4-4.

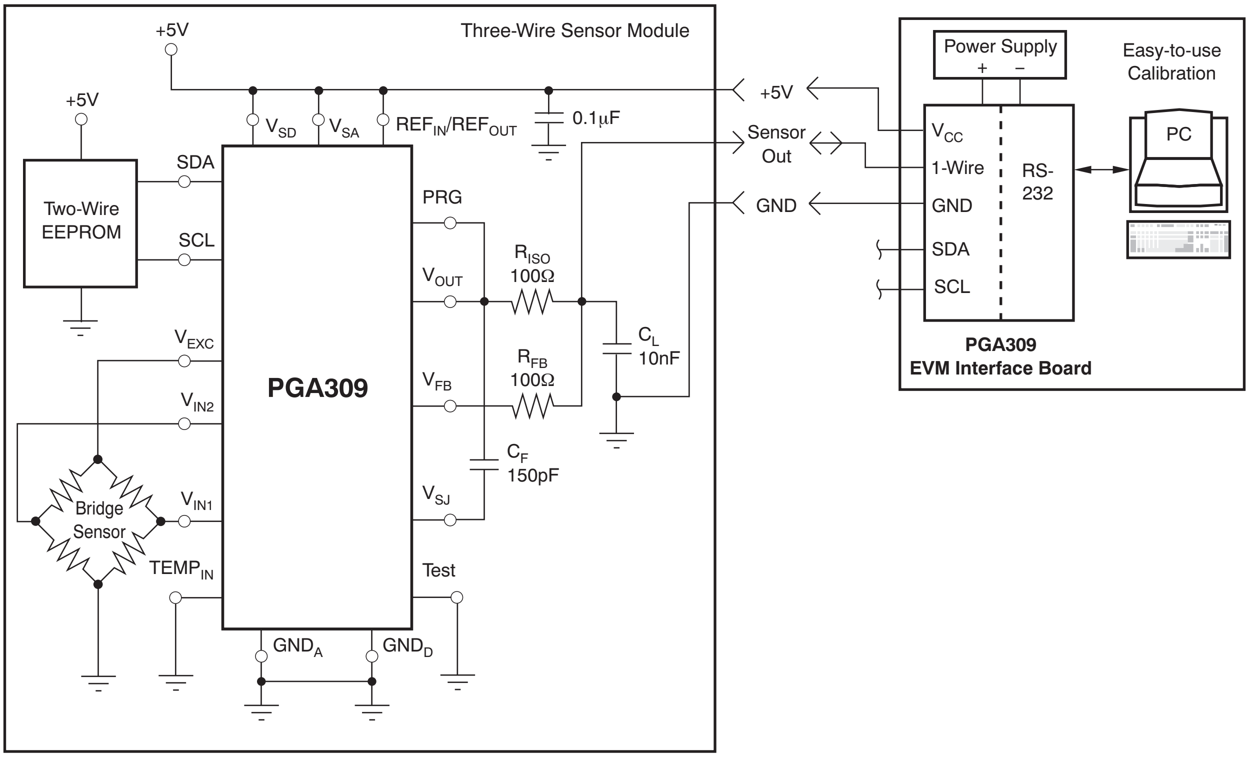


Figure 4-15. One-Wire Operation with PRG Tied to V_{OUT}

Table 4-3. Temp ADC—Delay After V_{OUT} Enable (Register 7)

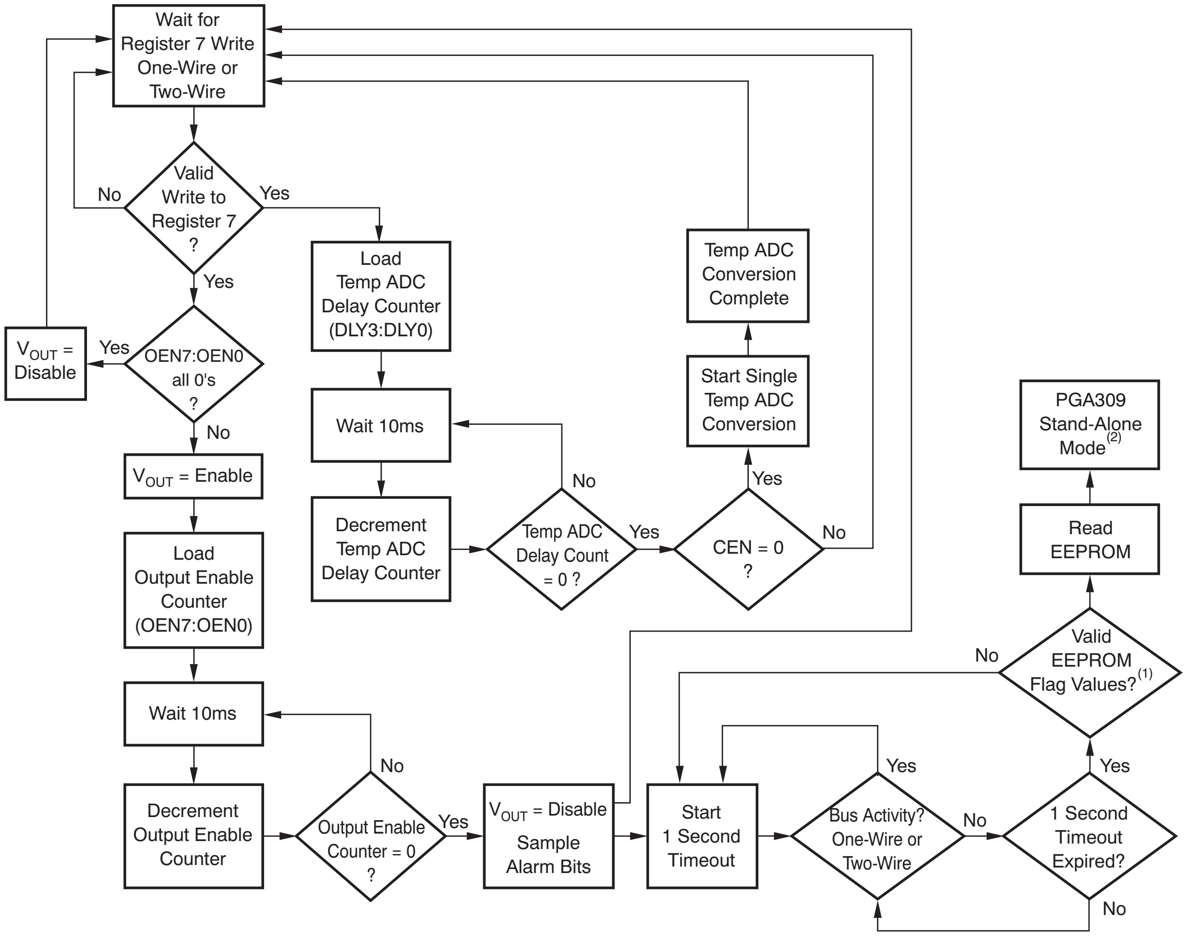
DLY3 [11]	DLY2 [10]	DLY1 [9]	DLY0 [8]	Decimal Equivalent (Initial Counter Value)	Temp ADC Delay (ms) [1]
0	0	0	0	0	0
0	0	0	1	1	10
0	0	1	0	2	20
0	0	1	1	3	30
0	1	0	0	4	40
0	1	0	1	5	50
0	1	1	0	6	60
0	1	1	1	7	70
1	0	0	0	8	80
1	0	0	1	9	90
1	0	1	0	10	100
1	0	1	1	11	110
1	1	0	0	12	120
1	1	0	1	13	130
1	1	1	0	14	140
1	1	1	1	15	150

[1] Temp ADC delay = intial counter value x 10ms.

Table 4-4. Output Enable Counter for One-Wire Interface/V_{OUT} Multiplexed Mode (Register 7)

Digital In put (Binary) OEN7......OEN0 [7......0]	Decimal Equivalent (Initial Counter Value)	V_{OUT} Enable Timeout (ms)
0000 0000	0	0 (V_{OUT} Disabled)
0010 0000	32	320
0100 0000	64	640
0110 0000	96	960
1000 0000	128	1280
1010 0000	160	1600
1100 0000	192	1920
1110 0000	224	2240
1111 1111	255	2550

Figure 4-16 details the output enable/disable state machine. Upon initial POR, there is a 25ms wait for communication through either digital interface to prevent the PGA309 from going through its POR sequence and reaching Stand-Alone Mode. The output enable/disable state machine can be forced to run at any time the PGA309 is powered and either digital interface (One-Wire or Two-Wire) can write to Register 7. Writing a non-zero value to OEN7:OEN0 will cause V_{OUT} to be immediately enabled and the Output Enable Counter to be loaded with the OEN7:OEN0 value (decimal equivalent x 10ms = initial Output Enable Counter value). V_{OUT} remains enabled until this initial Output Enable Counter value is decremented to 0 by 10ms increments. V_{OUT} is then disabled and a one second timeout begins waiting for bus activity on either digital interface (PRG pin for three-wire sensor application). As long as there is activity on the PRG pin, the one second timeout will be continually reset. After one second of no bus activity, the PGA309 stops and the state machine will try to read the EEPROM. It is important to store invalid data in the programmed flag values of the EEPROM for this calibration process, to prevent it from being read, which could change the register settings in the PGA309. This will also force the one second timeout to be reset and allow as long as needed for communication to start and stop on PRG. Once all registers in the PGA309 have been set to their desired values, another write to Register 7 will start the process all over again so a new analog value of V_{OUT} can be measured.



NOTE:

1. For calibration using PRG tied to V_{OUT}, set EEPROM programmed flag values to invalid values to prevent PGA309 registers from having their values changed by EEPROM register configuration and lookup table data.
2. In PGA309 Stand−Alone mode, if OWD (Register 4 [15]) is set to '1' in the first part of EEPROM (configuration part), then the One−Wire interface is disabled and the only way to communicate over the One−Wire interface is to cycle power on the PGA309 and begin communication over the One−Wire interface within 25ms of power on.

Figure 4-16. Output Enable/Disable State Machine

The second part of the output enable/disable state machine is the Temp ADC delay. During calibration, the Temp ADC conversion results will be needed at different calibration temperatures. These readings combined with measured V_{OUT} at the respective calibration temperatures are used to calculate the final temperature coefficients to be stored in the Lookup Table part of the external EEPROM. To use this function, the Temp ADC must be set to Single Start Convert mode (CEN = 0, Register 6 [10]). After a write to Register 7, the Temp ADC delay counter is loaded with the DLY3:DLY0 value (decimal equivalent x 10ms = initial Temp ADC delay counter value). This initial Temp ADC delay counter value is decremented to 0 by 10ms increments. When it reaches 0, a single Temp ADC conversion is triggered. No additional write to Register 6 [12] (the ADCS bit) is needed to initiate the conversion. Upon completion of the conversion, this branch of the state machine returns to waiting for the next valid Register 7 write.

The output enable/disable state machine allows three-wire sensor applications to measure temperature through the PGA309, against the calibration standard, for the PGA309 + sensor combination. It also allows PGA309 + sensor characteristics over pressure and temperature to be measured through the PGA309. These real-world results allow for accurate calculation of temperature coefficients for the Lookup Table and, therefore, accurate PGA309 + sensor digital calibration on a module-by-module basis.

The values of the Fault Monitor Alarm bits are latched immediately before the output is disabled to allow their values to be read through the One-Wire interface during factory calibration.

Once the final values are to be programmed into the EEPROM, it is desirable to have the One-Wire Interface disabled in three-wire sensor applications. This prevents V_{OUT} changes in the final end-use from being read back into the PGA309 through the One-Wire interface (PRG pin) and potentially misinterpreted as bus activity, which could then cause V_{OUT} to become disabled. To disable the One-Wire Interface, set the OWD bit to ‘1’ during the final EEPROM program write. The OWD (One-Wire Disable) bit is located in Register 4 [15]. After this final programming, the only way to communicate to the One-Wire Interface (PRG pin) is to cycle power on the PGA309 and begin communication within 33ms.

4.11 Four-Wire Modules and One-Wire Interface (PRG)

In four-wire module applications, it is essential that the OWD Bit (Register 4 [D15]) be set to '1' to disable the One-Wire interface after final programming is complete and before the final sensor module is sent out to the end application. In a four-terminal module, the PRG pin is connected directly to the outside world and is even more susceptible to noise coupled into it from periodic noise generators. Repetitive noise, such as a commutating motor or a switching power supply, can cause the PRG circuitry to misinterpret this noise as valid communication and put the PGA309 into an unpredicted state or, worse, cause EEPROM corruption.

Even if the OWD bit is set to '1' to disable the One-Wire interface, a 33ms window remains open on power-up, where periodic noise can be coupled into the PRG pin and be interpreted as coherent communication. The four-terminal module application, as show in Figure 4-17, requires detailed discussion and consideration when bringing the PRG pin directly to the outside world.

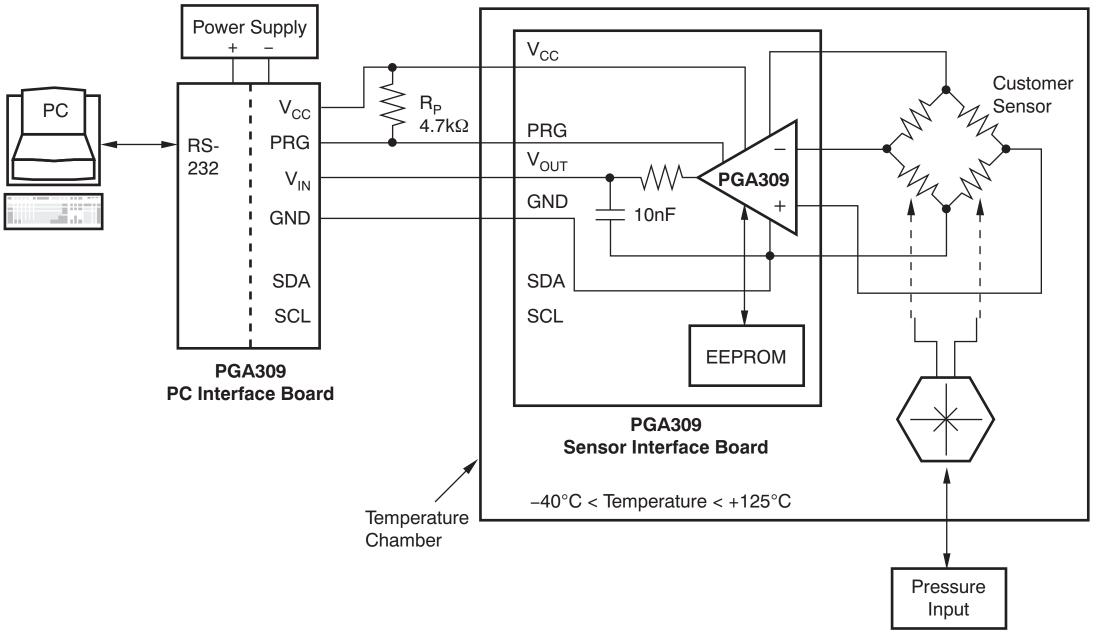


Figure 4-17. Four-Wire Sensor Module Application

Figure 4-20 depicts details of the PRG circuitry within the PGA309. Additional external protection components and electromagnetic interferences/radio frequency interference (EMI/RFI) filtering are included in this discussion. Considerations for programming the PGA309 four-terminal sensor module are presented with reference to Figure 4-20.

The PGA309 contains electrostatic discharge (ESD) cells, D2 and D1/SCR1, on the PRG pin to prevent ESD damage when the device is being handled before installation on a printed circuit board. These same ESD cells may not be adequate when the PGA309 is installed in a complete circuit with regards to electrical overstress. The ESD diodes D1 and D2 can handle up to 10mA continuous load. However, SCR1 will trigger with a 14V level and then drop to 3V at 80mA of sustaining current, as Figure 4-18 shows. If the current is not limited, the voltage will increase again; this increase, combined with higher currents, may cause permanent damage to the ESD cells and make the PRG circuitry unusable.

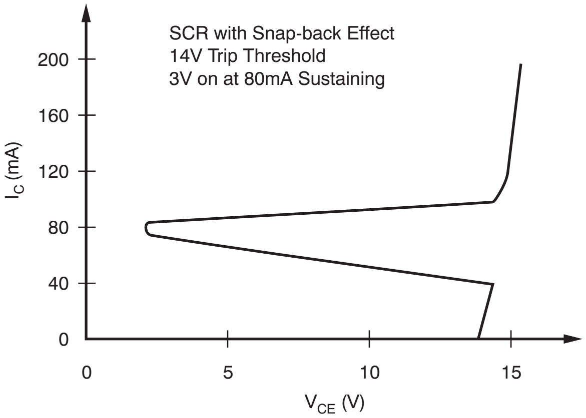


Figure 4-18. SCR ESD Cell

If miswiring is or external electrical overstresses are anticipated, the PRG pin must be protected by using external devices. SD1 and SD2 are signal Schottky diodes that steer current away from the internal ESD cells on the PRG pin during electrical overstress events. R7 will limit the current through SD1 and SD2. Z1 is a zener diode to clamp the energy passed through SD1. The selection of R7 can impact the valid logic levels at PRG_PGA309 and PRG_ Programmer. SW1 and R_{ON} represent the MOSFET switch and on-resistance used on the PGA309EVM or customer programmer that configures and calibrates the PGA309 over the One-Wire interface. For the PGA309, logic high is $0.7V_{SD}$ (3.5V for V_{SD} = 5V) or greater; logic low is $0.2V_{SD}$ (1V for V_{SD} = 5V) or less. Logic high is not a concern because there are pull-up resistors on the PGA309 module and on the programmer. The worst-case condition for logic low is shown in Figure 4-20; this figure illustrates the condition at approximately 610mV, which is less than the specified $0.2V_{SD}$ (1V for V_{SD} = 5V) maximum logic low. This configuration will be adequate for up to ±50V of miswiring on the 1W pin, based on current flow and the power dissipation of the components shown up to a temperature of +75°C.

Each individual application should be analyzed for electrical overstress and proper programming logic levels on the PRG pin.

Refer to Figure 4-21 for an illustration of common EMI/RFI filtering and the PRG pin configuration. Most EMI/RFI filter schemes typically involve connecting the chassis ground to the signal ground via capacitors in the range of 1nF to 10nF. These capacitors are connected on every pin into and out of the module. In Figure 4-21, we connect the signal ground to the chassis ground with capacitor C2 (1nF). V_{CC} is connected to the chassis ground through capacitor C4 (100nF) and capacitor C2 (1nF). We also add capacitor C1 (10nF) from the PRG pin at the module output and tie it directly to V_{CC}. This configuration is optimal for rejecting any switching disturbances between the chassis ground and the signal ground.

EMI/RFI is often seen as disturbance referenced to the chassis ground, as shown in Figure 4-19. A common source impedance of 50Ω (through R11) is assumed. The disturbance is injected into the PRG pin of the module, and will then flow through capacitors C3 (10nF), C4 (100nF), and C2 (1nF) as it returns to chassis ground. A severe disturbance of ±5V at 100kHz will only degrade the logic high voltage on the PRG pin from 5V to 4.27V, as shown in Figure 5-4. The minimum logic high is $0.7V_{SD}$ (3.5V for V_{SD} = 5V) , and thus there will be no PRG miscommunication caused by this severe disturbance between chassis ground and signal ground.

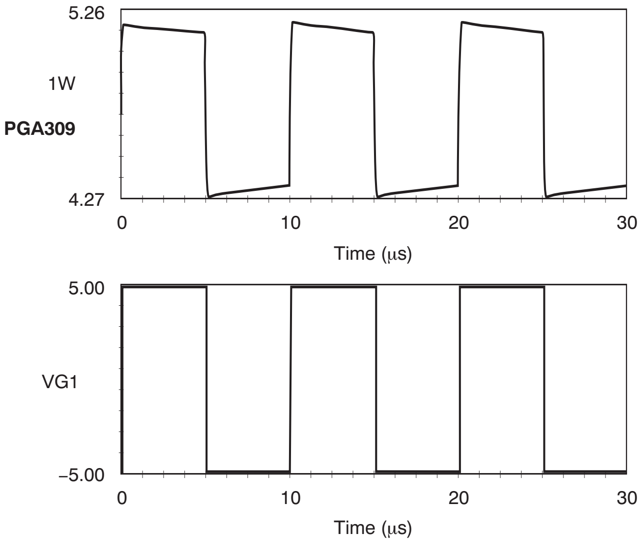


Figure 4-19. Severe EMI/RFI Disturbance

As a final note, consider Figure 4-20 once more, and observe that in order to program a PRG pin on a module with large capacitance (for example, with C1 = 10nF) on the PRG pin, the customer programmer must use a PRG speed-up circuit, which detects a rising edge on the PRG signal. Based on this rising edge, a switch connects the PRG line to +5V through a 200Ω resistor for 5µs in order to quickly charge capacitor C1 (10nF) and obtain a reasonable rising edge in logic '0' to logic '1' transitions. The PGA309EVM has this PRG speed-up circuit already installed in the PC Programmer Interface Board.

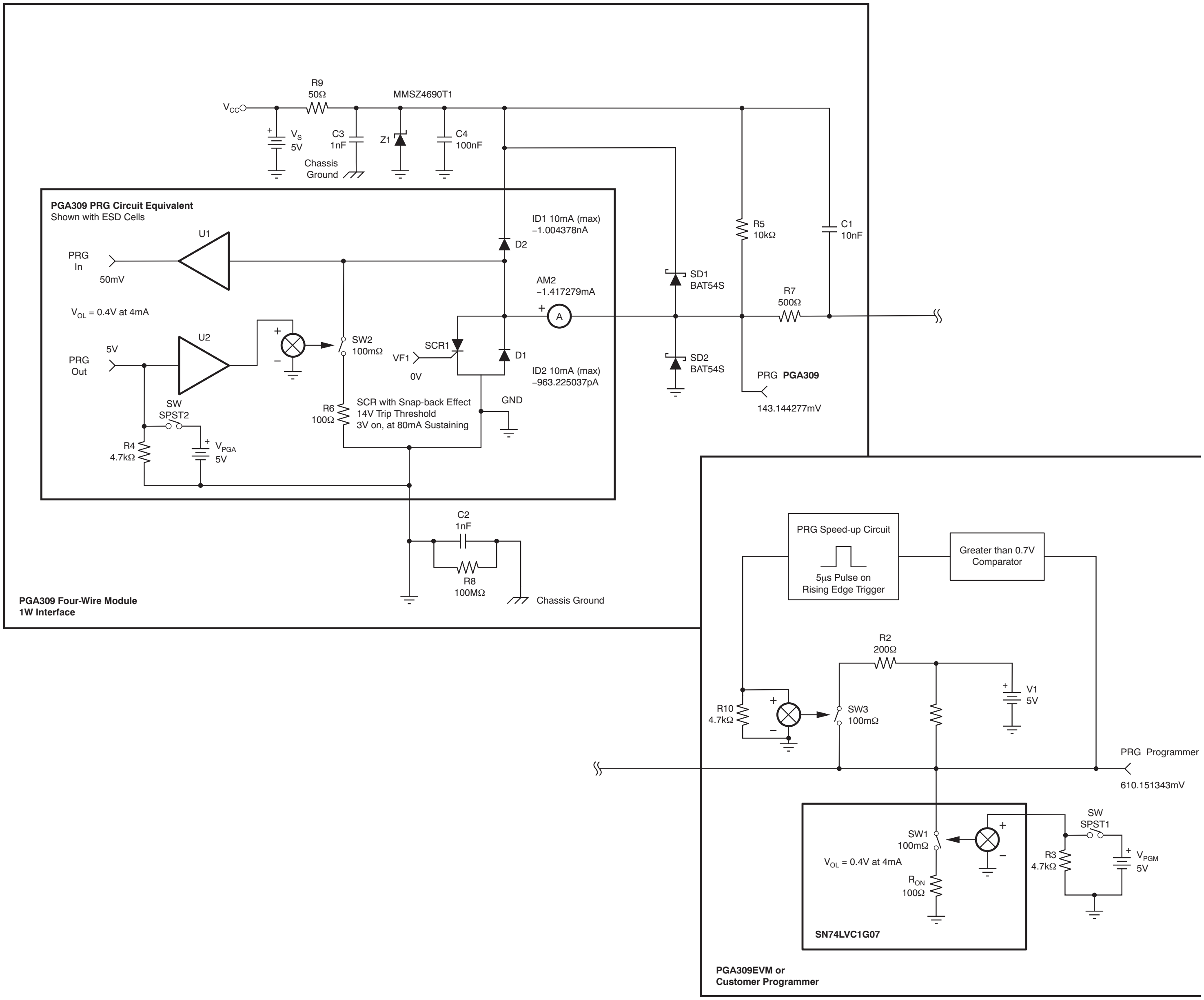


Figure 4-20. PRG Circuit Protection Logic Levels

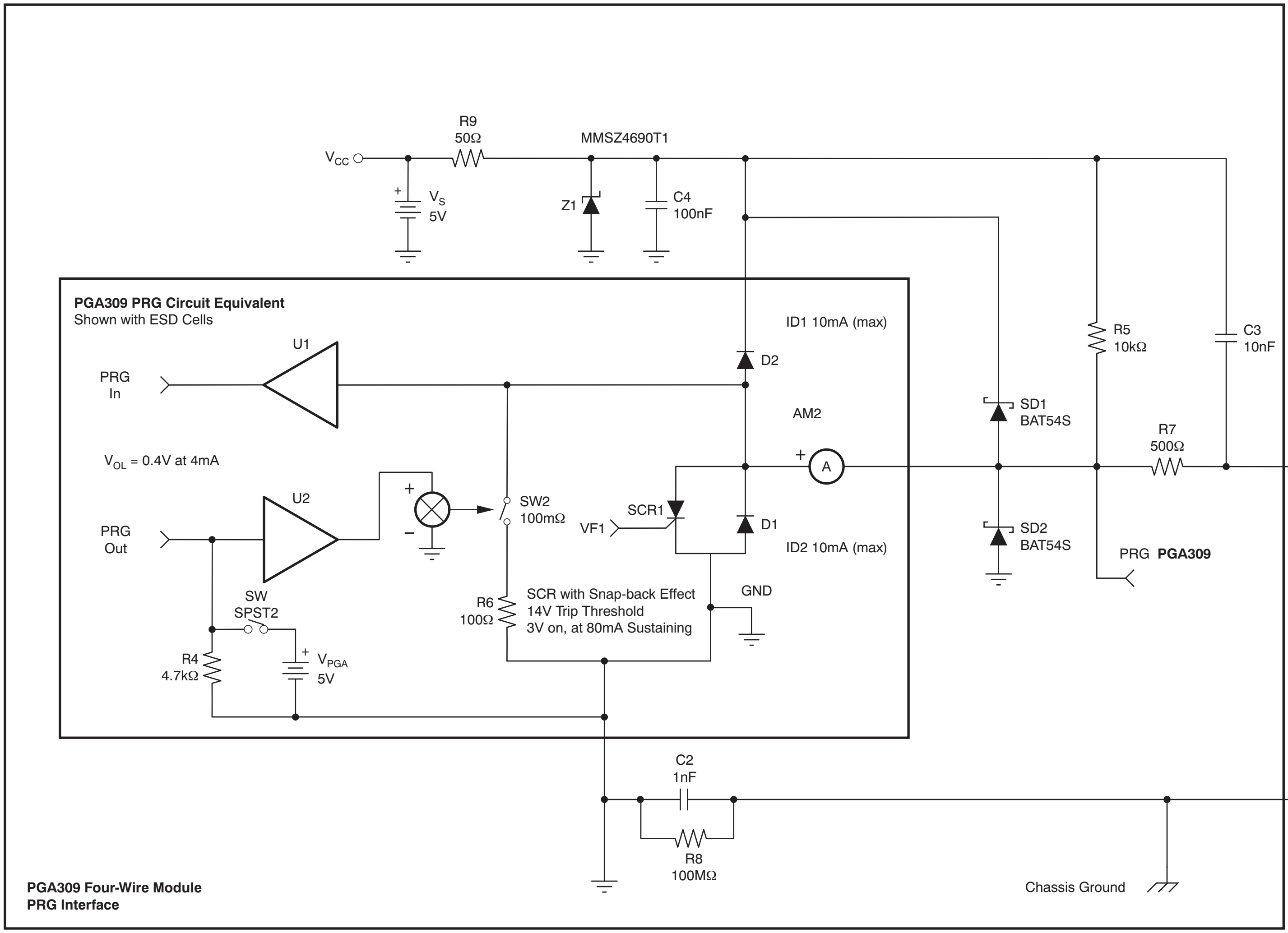


Figure 4-21. PRG Circuit EMI/RFI Filtering

Application Background

This chapter describes the application background of the PGA309.

Topic **Page**

5.1 Bridge Sensors

A typical bridge pressure sensor is shown in Figure 5-1. For a given bridge excitation voltage (V_{EXC}), the output voltage of the bridge ($V_P - V_N$) is a voltage proportional to the pressure applied to the sensor.

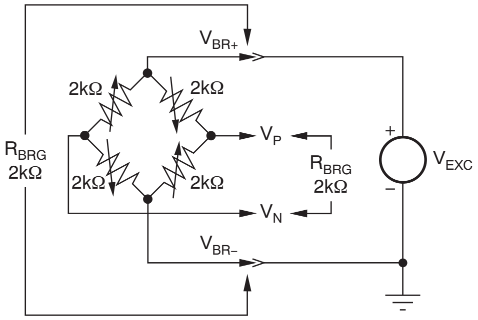


Figure 5-1. Typical Bridge Sensor

Span is the scale factor for $V_P - V_N$ at full-scale pressure input relative to the bridge excitation ($V_{BR+} - V_{BR-}$). Span is also called FSO (Full-Scale Output), FSS (Full-Scale Sensitivity), Sensitivity, or Gain. For example, with a bridge excitation voltage of 5V, a 2mV/V FSS implies that the bridge output will be 10mV at full-scale pressure.

Offset, also known as Zero, is the output of the bridge ($V_P - V_N$) with zero pressure applied. Often a bridge sensor's Zero may be equal to or greater than its FSS for a given excitation voltage. Figure 5-2 graphically illustrates the definition of Span and Offset.

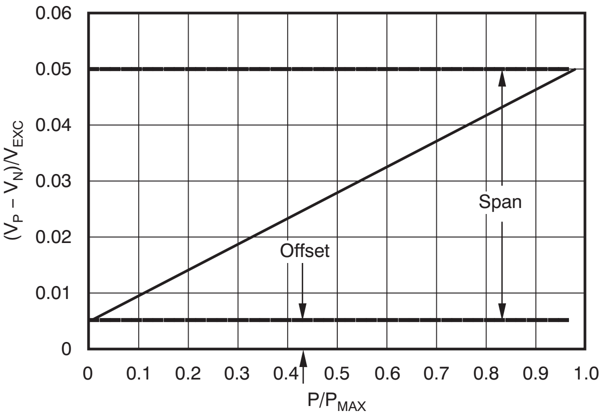


Figure 5-2. Example of Span and Offset

An ideal sensor would have span and offset curves over temperature, as shown in Figure 5-3. Real-world sensors have span and offset changes that change over temperature. Both span and offset have variations at +25°C, linear changes with temperature, and nonlinear changes with temperature. Figure 5-4 and Figure 5-5 illustrate span and offset changes over temperature for a bridge sensor with second-order nonlinearities. TC1 coefficients represent a linear change with temperature, and TC2 a second-order change with temperature.

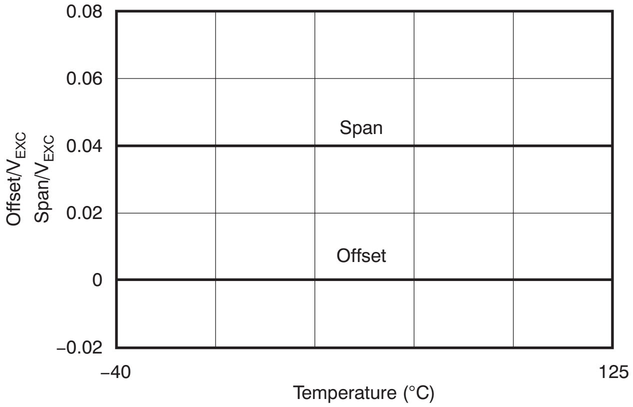


Figure 5-3. Ideal Span and Offset vs Temperature

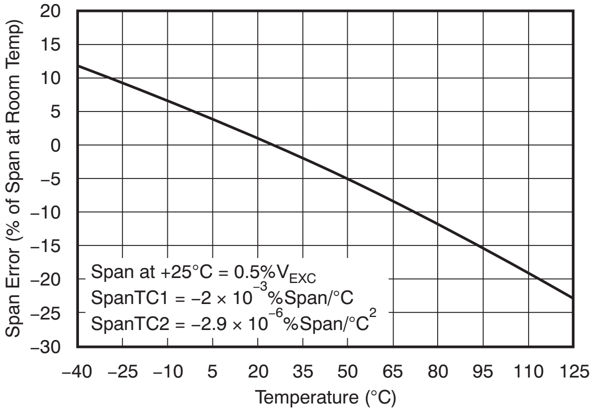


Figure 5-4. Effect of Nonlinearity on Bridge Sensor Span Over Temperature

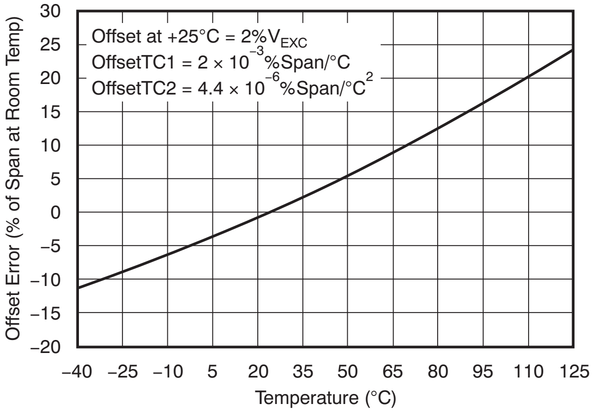


Figure 5-5. Effect of Nonlinearity on Bridge Sensor Offset Over Temperature

Many bridge sensors have a nonlinear output with applied pressure. Figure 5-6 shows the non-ideal curves for both a positive and negative nonlinear bridge sensor output with applied pressure. The PGA309 provides calibration over temperature for both span and offset, and has dedicated linearization circuitry to linearize many types of bridge sensors whose outputs are not linear with applied pressure.

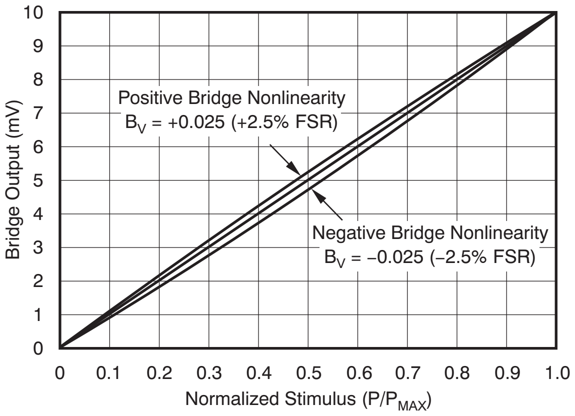


Figure 5-6. Non-Ideal Curves for Both a Positive and Negative Nonlinear Bridge Sensor Output with Applied Pressure

5.2 System Scaling Options for Bridge Sensors

There are two system scaling options for bridge sensor outputs: Absolute Scale and Ratiometric Scale.

5.2.1 Absolute Scale

Absolute Scale scales the output range as a percentage of a reference voltage, V_{REF}. For example, the absolute-scaled output of a bridge sensor can be set to the range of 10% to 90% of V_{REF}. Figure 5-7 illustrates such a case.

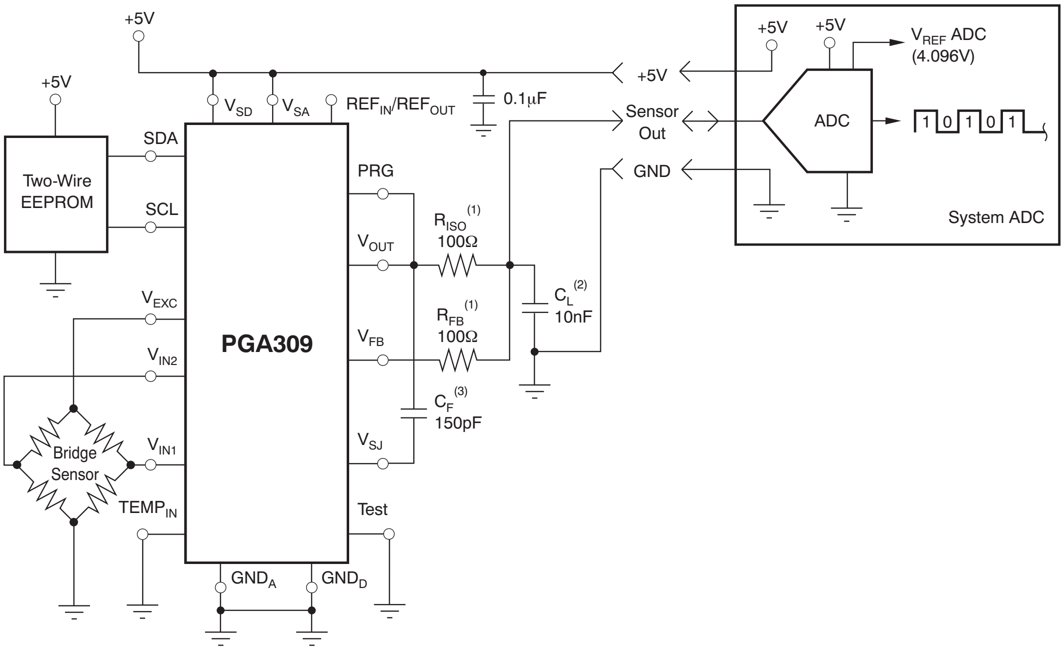


Figure 5-7. Absolute Scaling Conditions

5.2.2 Ratiometric Scale

Ratiometric Scale scales the output range as a percentage of the supply voltage. For example, the ratiometric-scaled output of a bridge sensor can be set to the range of 10% to 90% of V_S, shown in Figure 5-8. Figure 5-9 shows that as the supply voltage, V_S, is lowered from +5V to +3V the range for V_{OUT} of 10% to 90% of V_S remains the same. The PGA309 accommodates both Absolute and Ratiometric scaling of bridge sensors.

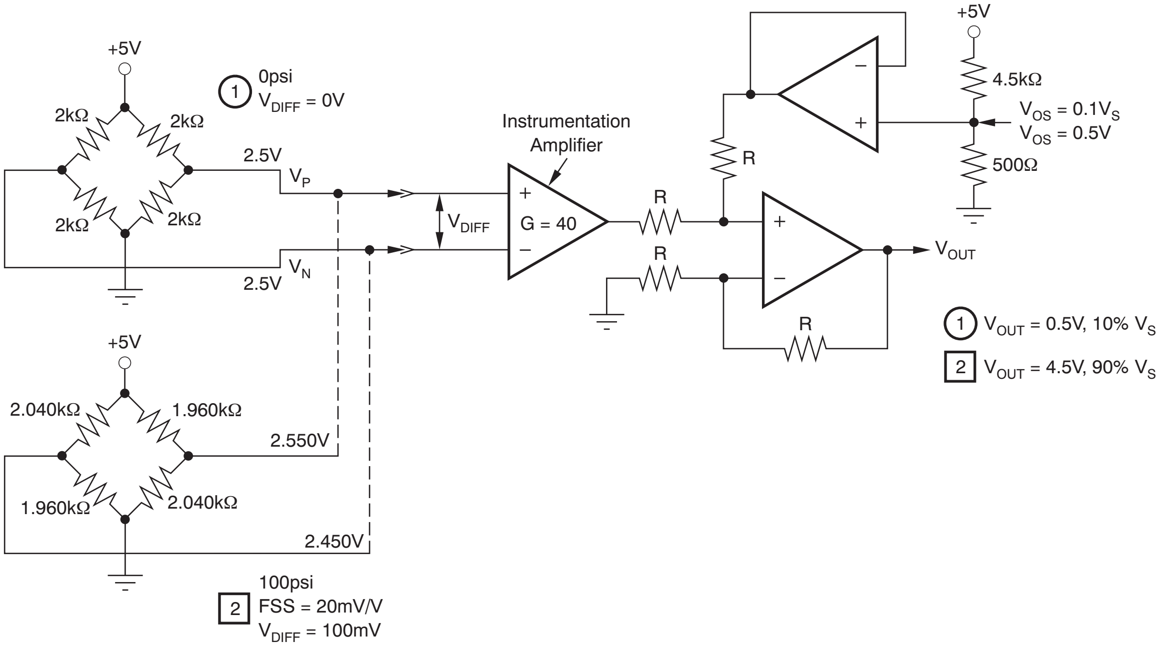


Figure 5-8. Ratiometric Configuration, 5V

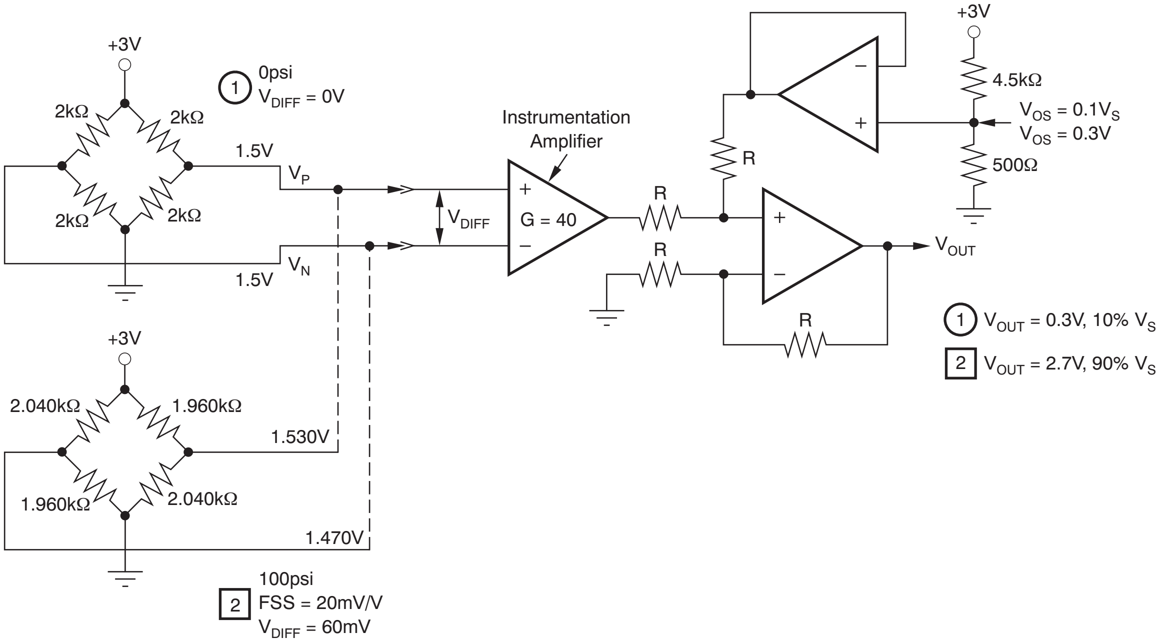


Figure 5-9. Ratiometric Configuration, 3V

5.3 Trimming Real World Bridge Sensors for Linearity

Traditional methods for trimming nonlinear, real-world bridge sensors to a linear, useful function require additional resistors to be added around the base bridge sensor, as shown in Figure 5-10. This approach often requires special prepackaged fixtures and special laser trim or manual trim resistors. The trims are interactive with each other, which requires multiple test/trim/test/trim passes; this only allows for a finite number of trims and range for a particular bridge sensor.

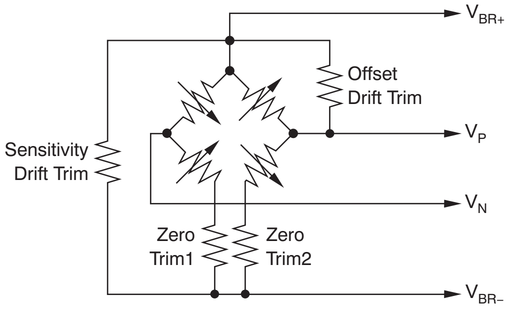


Figure 5-10. Typical Trim Configuration

The PGA309 provides a modern digital trim approach for bridge sensors, as shown in Figure 5-11. This technique allows for post-package trim of both the bridge sensor and its signal conditioning electronics. The digital trimming is simplified through the use of a computer interface and spreadsheet analysis computation tools. A near-infinite number of trim cycles can be performed with finer resolution, wider range, and less interaction between trimmed parameters than the traditional trim method. Packaging shifts are eliminated.

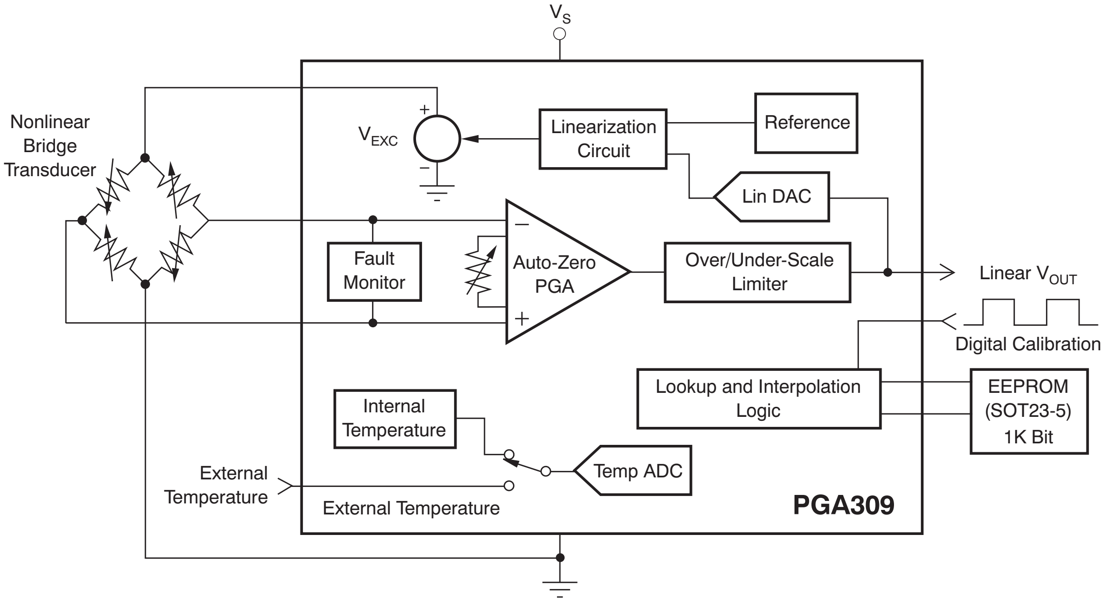


Figure 5-11. PGA309 Trim Configuration

Register Descriptions

This chapter describes the PGA309 registers and their contents.

Topic **Page**

6.1 Internal Register Overview

Table 6-1. Internal Register Overview

Address Pointer					Register Description	Type [1]	Register Controls
P4	**P3**	**P2**	**P1**	**P0**			
0	0	0	0	0	Register 0—Temp ADC Output	R	Temp ADC Output Data
0	0	0	0	1	Register 1—Fine Offset Adjust (Zero DAC)	R/W	Fine Offset Adjust (Zero DAC) Setting
0	0	0	1	0	Register 2—Fine Gain Adjust (Gain DAC)	R/W	Fine Gain Adjust (Gain DAC) Setting
0	0	0	1	1	Register 3—Reference Control and Linearization Register	R/W	Reference Configuration Settings; V_{EXC} Enable; Linearization Setting
0	0	1	0	0	Register 4—Front End PGA Coarse Offset Adjust and Gain Select; Output Amplifier Gain Select	R/W	Front End PGA Coarse Offset Setting; PGA Gain Select; Output Amplifier Gain Select; One-Wire Disable
0	0	1	0	1	Register 5—PGA Configuration and Over/Under Scale Limit	R/W	Over/Under Scale Limits, Polarities, Enable; Fault Comparator Select
0	0	1	1	0	Register 6—Temp ADC Control Register	R/W	Temp ADC Conversion Speed, Ref Select; Int/Ext Temp Mode Select; Ext Temp PGA Configuration; $TEMP_{IN}$ Current Source Enable
0	0	1	1	1	Register 7—Output Enable Counter Control	R/W	Temp ADC Delay Setting; One-Wire Interface Output Enable Setting
0	1	0	0	0	Register 8—Alarm Status	R	Fault Monitor Comparator Outputs

[1] Type: R = Read-only, R/W = Read/Write

6.2 Internal Register Map

6.2.1 Register 0: Temp ADC Output Register (Read Only, Address Pointer = 00000)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

AD[15:0] Temp ADC Output

Internal Temperature Mode: 12-bit + sign extended, right justified, Twos Complement data format
External Temperature Mode: 15-bit + sign extended, right-justified, Twos Complement data format

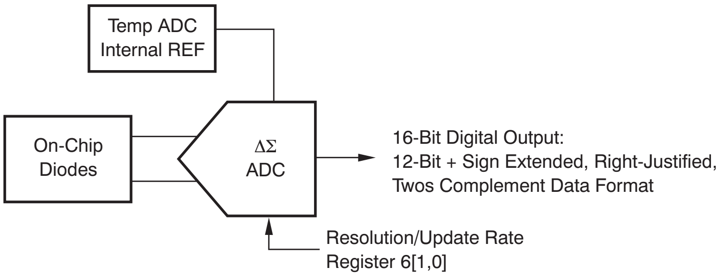


Figure 6-1. Internal Temperature Mode; Register 6[9] = '1'

Table 6-2. Internal Temperature Mode−Data Format (12-Bit Resolution). TEN = 1; R1, R0 = ‘11’[1]

Temperature (°C)	Digital Output AD15............AD0 (Binary)	Digital Output (Hex)
150	0000 1001 0110 0000	960
128	0000 1000 0000 0000	800
127.9375	0000 0111 1111 1111	07FF
100	0000 0110 0100 0000	640
80	0000 0101 0000 0000	500
75	0000 0100 1011 0000	04B0
50	0000 0011 0010 0000	320
25	0000 0001 1001 0000	190
0.25	0000 0000 0000 0100	4
0	0000 0000 0000 0000	0
−0.25	1111 1111 1111 1100	FFFC
−25	1111 1110 0111 0000	FE70
−55	1111 1100 1001 0000	FC90

---

[1] The resolution for the Temp ADC in Internal Temperature Mode is 0.0625°C/count.
For positive temperatures (for example, +50°C):
(50°C)/(0.0625°C/count) = 800 → 320h → 0011 0010 0000
50°C will be read by the Temp ADC as 0000 0011 0010 0000 → 0320h
For negative temperatures (for example, −25°C):
(|[−25]|)/(0.0625°C/count) = 400 → 190h → 0001 1001 0000
Convert to Twos Complement notation.
−25°C will be read by the Temp ADC as 1111 1110 0111 0000 → FE70h

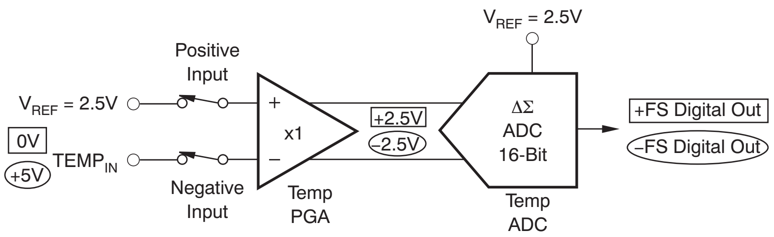


Figure 6-2. External Signal Mode; Register 6 = ‘0000 0100 0011 0000’

Table 6-3. External Signal Mode—Data Format Example (Register 6 = ‘0000 0100 0011 0011’), 15-Bit + Sign Resolution. REN = 1, RS = 1

TEMP_{IN} (V)	Temp ADC Input (V)	Temp ADC Input (Ratio to Full Scale) [1]	Digital Output AD15............AD0 (Binary)	Digital Output (Hex)
0.0001	2.49992371	+0.999969 V_{REFT}	0111 1111 1111 1111	7FFF
+0.625	+1.875	+0.75 V_{REFT}	0110 0000 0000 0000	6000
+1.25	+1.25	+0.5 V_{REFT}	0100 0000 0000 0000	4000
+1.925	+0.575	+0.23 V_{REFT}	0001 1101 0111 0001	1D71
+2.4999	+0.00007629	+(1/32768) V_{REFT}	0000 0000 0000 0001	0001
+2.5	0	+0 V_{REFT}	0000 0000 0000 0000	0000
+2.50007629	−0.00007629	−(1/32768) V_{REFT}	1111 1111 1111 1111	FFFF
+3.075	−0.575	−0.23 V_{REFT}	1110 0010 1000 1111	E28F
+3.75	−1.25	−0.5 V_{REFT}	1100 0000 0000 0000	C000
+4.375	−1.875	−0.75 V_{REFT}	1010 0000 0000 0000	A000
+5	−2.5	−1 V_{REFT}	1000 0000 0000 0000	8000

---

[1] V_{REFT} can be V_{SA}, V_{EXC}, or V_{REF}.

6.2.2 Register 1: Fine Offset Adjust (Zero DAC) Register (Read/Write, Address Pointer = 00001)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
POR Value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

ZD[15:0]: Zero DAC control, 16-bit unsigned data format

Table 6-4. Zero DAC—Data Format Example (V_{REF} = +5V)

Digital Input (Hex)	Digital Input ZD15............ZD0 (Binary)	Zero DAC Output (V)	Zero DAC Output
0000	0000 0000 0000 0000	0	0 V_{REF}
0001	0000 0000 0000 0001	0.00007629	(1/65536) V_{REF}
051F	0000 0101 0001 1111	0.100021362	0.02 V_{REF} (1)
4000	0100 0000 0000 0000	1.25	0.25 V_{REF}
8000	1000 0000 0000 0000	2.5	0.50 V_{REF}
C000	1100 0000 0000 0000	3.75	0.75 V_{REF}
FAE1	1111 1010 1110 0001	4.899978638	0.98 V_{REF} (1)
FFFF	1111 1111 1111 1111	4.999923706	0.9999847 V_{REF}

(1) Ensured by design Zero DAC Range of Adjustment (0.02V_{REF} to 0.98V_{REF})

Zero DAC Equation:

Decimal # Counts = ($V_{ZERO\ DAC}$/V_{REF})(65536)
$0.1V \leq$ Zero DAC Analog Range $\leq V_{SA} - 0.1V$
$0 \leq$ Zero DAC Programming Range $\leq V_{REF}$

Zero DAC Example:

Want: $V_{ZERO\ DAC}$ = 0.5V
Given: V_{REF} = 5V
Decimal # Counts = 0.5 / (5/65536) = 6553.6
Use 6554 counts → 199Ah → 0001 1001 1001 1010

6.2.3 Register 2: Fine Gain Adjust (Gain DAC) Register (Read/Write, Address Pointer = 00010)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	GD15	GD14	GD13	GD12	GD11	GD10	GD9	GD8	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0
POR Value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

GD[15:0]: Gain DAC control, 16-bit unsigned data format

Table 6-5. Gain DAC—Data Format

Digital Input (Hex)	Digital Input ZD15...........ZD0 (Binary)	Gain Adjust
0000	0000 0000 0000 0000	0.333333333
0001	0000 0000 0000 0001	0.333343505
32F2	0011 0010 1111 0010	0.466003417
4000	0100 0000 0000 0000	0.500000000
6604	0110 0110 0000 0100	0.598999023
9979	1001 1001 0111 1001	0.733001708
CC86	1100 1100 1000 0110	0.865997314
FFFF	1111 1111 1111 1111	1.000000000

Gain DAC Equation:

1 LSB = (1.000000000 – 0.333333333) / 65536 = (2/3)/65536
Decimal # Counts = (Desired Gain – 1/3)/(3/2)(65.536)
0.3333333 ≤ Gain DAC ≤ 0.9999898
0 ≤ Gain DAC Counts ≤ 65535

Gain DAC Example:

Want: Fine Gain = 0.68
Decimal # Counts = (0.68 − 1/3)(3/2)(65536) = 34078.72
Use 34079 counts → 851Fh → 1000 0101 0001 1111

6.2.4 Register 3: Reference Control and Linearization Register (Read/Write, Address Pointer = 00011)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RFB	RFB	RFB	RFB	EXS	EXEN	RS	REN	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: Reserved Factory Bit: Set to zero for proper operation

EXS: Linearization Adjust and Excitation Voltage (V_{EXC}) Gain Select (Range1 or Range2)

0 = Range 1 ($-0.166V_{FB}$ < Linearization DAC Range < $+0.166V_{FB}$, V_{EXC} Gain = $0.83V_{REF}$)
1 = Range 2 ($-0.124V_{FB}$ < Linearization DAC Range < $+0.124V_{FB}$, V_{EXC} Gain = $0.52V_{REF}$)

EXEN: V_{EXC} Enable

1 = Enable V_{EXC}
0 = Disable V_{EXC}

RS: Internal V_{REF} Select (2.5V or 4.096V)

0 = 4.096V
1 = 2.5V

REN: Enable/Disable Internal V_{REF} (disable for external V_{REF}—connect external V_{REF} to REFIN/REFOUT pin)

0 = External Reference (disable internal reference)
1 = Internal Reference (enable internal reference)

LD[7:0]: Linearization DAC setting, 7-bit + sign

Table 6-6. Linearization DAC—Data Format Example (Range 1: $-0.166V_{FB}$ < Linearization DAC Range < $+0.166V_{FB}$)

Digital Input (Hex)	Digital Input LD7......LD0	Linearization Adjust
FF	1111 1111	$-0.166\ V_{FB}$
E0	1110 0000	$-0.12548\ V_{FB}$
C0	1100 0000	$-0.08365\ V_{FB}$
A0	1010 0000	$-0.04183\ V_{FB}$
81	1000 0001	$-0.00131\ V_{FB}$
80	1000 0000	$0\ V_{FB}$
00	0000 0000	$0\ V_{FB}$
01	0000 0001	$+0.00131\ V_{FB}$
20	0010 0000	$+0.04183\ V_{FB}$
40	0100 0000	$+0.08365\ V_{FB}$
60	0110 0000	$+0.12548\ V_{FB}$
7F	0111 1111	$+0.166\ V_{FB}$

Linearization DAC Equation:

Decimal # Counts = |Desired V_{FB} Ratio| / (Full-Scale Ratio/127)

Linearization DAC Example:

Given: (Range 1: $-0.166V_{FB}$ < Linearization DAC Range < $+0.166V_{FB}$)
Want: V_{FB} Ratio = −0.082
Decimal # Counts = 0.082/(0.166/127) = 62.7349
Use 63 counts → 0x3F → 0011 1111
Add a ‘1’ in the Sign Bit (MSB, bit 7) to denote the negative ratio:
Final Linearization DAC Setting: 1011 1111 → BFh

6.2.5 Register 4: PGA Coarse Offset Adjust and Gain Select/Output Amplifier Gain Select Register (Read/Write, Address Pointer = 00100)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	0WD	GO2	GO1	GO0	GI3	GI2	GI1	GI0	RFB	RFB	RFB	OS4	OS3	OS2	OS1	OS0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

OWD: One-Wire Disable (only valid while V_{OUT} is enabled, for use when PRG is connected to V_{OUT})

1 = Disable
0 = Enable

GO[2:0]: Output Amplifier Gain Select, 1-of-7 plus internal feedback disable

GI[3:0]: Front-End PGA Gain Select, 1-of-8, and Input Mux Control

GI[3] = Input Mux Control
GI[2:0] = Gain Select

RFB: Reserved Factory Bit: Set to zero for proper operation

OS[4:0]: Coarse Offset Adjust on Front-End PGA, 4-bit + sign

1LSB = $(V_{REF})(0.85E - 3)$

Table 6-7. Output Amplifier—Gain Select

GO2 [14]	GO1 [13]	GO0 [12]	Output Amplifier Gain
0	0	0	2
0	0	1	2.4
0	1	0	3
0	1	1	3.6
1	0	0	4.5
1	0	1	6
1	1	0	9
1	1	1	Disable Internal Feedback

Table 6-8. Front End PGA—Gain Select

GI2 GAIN SEL2 [10]	GI1 GAIN SEL1 [9]	GI0 GAIN SEL0 [8]	Front-End PGA Gain
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	23.27
1	0	0	32
1	0	1	42.67
1	1	0	64
1	1	1	128

Table 6-9. Front End PGA—MUX Select

GI3 MUX CNTL	Input MUX State [1]
0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$
1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$

[1] V_{IN1} = Pin 4, V_{IN2} = Pin 5, V_{INP} = positive input to Front-End PGA, V_{INN} = negative input to Front-End PGA; see detailed block diagram (Figure B-1).

Table 6-10. Coarse Offset Adjust on Front-End PGA—Data Format Example (V_{REF} = +5V)

OS4 [4]	OS3 [3]	OS2 [2]	OS1 [1]	OS0 [0]	Coarse Offset (mV)	Coarse Offset
1	1	1	1	1	−59.5	$-14(V_{REF})(0.85E-3)$
1	1	1	1	0	−55.25	$-13\ (V_{REF})(0.85E-3)$
1	1	1	0	1	−51	$-12\ (V_{REF})(0.85E-3)$
1	1	1	0	0	−46.75	$-11\ (V_{REF})(0.85E-3)$
1	1	0	1	1	−42.5	$-10\ (V_{REF})(0.85E-3)$
1	1	0	1	0	−38.25	$-9\ (V_{REF})(0.85E-3)$
1	1	0	0	1	−34	$-8(V_{REF})(0.85E-3)$
1	1	0	0	0	−29.75	$-7\ (V_{REF})(0.85E-3)$
1	0	1	1	1	−29.75	$-7\ (V_{REF})(0.85E-3)$
1	0	1	1	0	−25.5	$-6\ (V_{REF})(0.85E-3)$
1	0	1	0	1	−21.25	$-5\ (V_{REF})(0.85E-3)$
1	0	1	0	0	−17	$-4\ (V_{REF})(0.85E-3)$
1	0	1	0	1	−12.75	$-3\ (V_{REF})(0.85E-3)$
1	0	0	1	0	−8.5	$-2\ (V_{REF})(0.85E-3)$
1	0	0	0	1	−4.25	$-1\ (V_{REF})(0.85E-3)$
1	0	0	0	0	0	$0V_{REF}$
0	0	0	0	0	0	$0V_{REF}$
0	0	0	0	1	+4.25	$+1\ (V_{REF})(0.85E-3)$
0	0	0	1	0	+8.5	$+2\ (V_{REF})(0.85E-3)$
0	0	0	1	1	+12.75	$+3\ (V_{REF})(0.85E-3)$
0	0	1	0	0	+17	$+4\ (V_{REF})(0.85E-3)$
0	0	1	0	1	+21.25	$+5\ (V_{REF})(0.85E-3)$
0	0	1	1	0	+25.5	$+6\ (V_{REF})(0.85E-3)$
0	0	1	1	1	+29.75	$+7\ (V_{REF})(0.85E-3)$
0	1	0	0	0	+29.75	$+7\ (V_{REF})(0.85E-3)$
0	1	0	0	1	+34	$+8\ (V_{REF})(0.85E-3)$
0	1	0	1	0	+38.25	$+9\ (V_{REF})(0.85E-3)$
0	1	0	1	1	+42.5	$+10\ (V_{REF})(0.85E-3)$
0	1	1	0	0	+46.75	$+11\ (V_{REF})(0.85E-3)$
0	1	1	0	1	+51	$+12\ (V_{REF})(0.85E-3)$
0	1	1	1	0	+55.25	$+13\ (V_{REF})(0.85E-3)$
0	1	1	1	1	+59.5	$+14\ (V_{REF})(0.85E-3)$

6.2.6 Register 5: PGA Configuration and Over/Under-Scale Limit Register (Read/Write, Address Pointer = 00101)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RFB	RFB	CLK_ CFG 1	CLK_ CFG 0	EXT EN	INT EN	EXT POL	INT POL	RFB	OU EN	HL2	HL1	HL0	LL2	LL1	LL0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: (Reserved Factory Bit): Set to zero for proper operation

CLK_CFG[1:0]: Clocking scheme for Front-End PGA auto-zero and Coarse Offset DAC Chopping

EXTEN: Enable External Fault Comparator Group (INP_HI, INP_LO, INN_LO, INN_HI)

1 = Enable External Fault Comparator Group
0 = Disable External Fault Comparator Group

INTEN: Enable Internal Fault Comparator Group (A2SAT_LO, A2SAT_HI, A1SAT_LO, A1SAT_HI, A3_VCM)

1 = Enable Internal Fault Comparator Group
0 = Disable Internal Fault Comparator Group

EXTPOL: Selects V_{OUT} output polarity when External Fault Comparator Group detects a fault, if EXTEN = 1

1 = Force V_{OUT} high when any comparator in the External Fault Comparator Group detects a fault
0 = Force V_{OUT} low when any comparator in the External Fault Comparator Group detects a fault

INTPOL: Selects V_{OUT} output polarity when Internal Fault Comparator Group detects a fault, if INTEN = 1

1 = Force V_{OUT} high when any comparator in the Internal Fault Comparator Group detects a fault
0 = Force V_{OUT} low when any comparator in the Internal Fault Comparator Group detects a fault

OUEN: Over/Under-Scale Limit Enable.

1 = Enable Over/Under-Scale limits
0 = Disable Over/Under-Scale limits

HL[2:0]: Over-Scale Threshold Select

LL[2:0]: Under-Scale Threshold Select

Table 6-11. Clock Configuration (Front End PGA Auto-Zero and Coarse Adjust DAC Chopping)

ClK_CFG1 [13]	CLK_CFG0 [12]	PGA Front End Auto-Zero	Coarse Adjust DAC Chopping
0	0	7kHz typical	3.5kHz typical
0	1	7kHz typical	Off (none)
1	0	7kHz typical, Random Clocking	3.5kHz typical, Random Clocking
1	1	7kHz typical	3.5kHz typical, Random Clocking

Table 6-12. Over-Scale Threshold Select (V_{REF} = +5V)

HL2 [5]	HL1 [4]	HL0 [3]	Over-Scale Threshold (V)	Over-Scale Threshold
0	0	0	4.854	0.9708 V_{REF}
0	0	1	4.805	0.9610 V_{REF}
0	1	0	4.698	0.9394 V_{REF}
0	1	1	4.580	0.9160 V_{REF}
1	0	0	4.551	0.9102 V_{REF}
1	0	1	3.662	0.7324 V_{REF}
1	1	0	2.764	0.5528 V_{REF}
1	1	1	Reserved	—

Table 6-13. Under-Scale Threshold Select (V_{REF} = +5V)

LL2 [2]	LL1 [1]	LL0 [0]	Under-Scale Threshold (V)	Under-Scale Threshold
0	0	0	0.127	0.02540 V_{REF}
0	0	1	0.147	0.02930 V_{REF}
0	1	0	0.176	0.03516 V_{REF}
0	1	1	0.196	0.03906 V_{REF}
1	0	0	0.225	0.04492 V_{REF}
1	0	1	0.254	0.05078 V_{REF}
1	1	0	0.274	0.05468 V_{REF}
1	1	1	0.303	0.06054 V_{REF}

6.2.7 Register 6: Temp ADC Control Register (Read/Write, Address Pointer = 00110)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RFB	RFB	ADC2X	ADCS	ISEN	CEN	TEN	AREN	RV1	RV0	M1	M0	G1	G0	R1	R0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: Reserved Factory Bit: Set to zero for proper operation

ADC2X: Temp ADC runs 2x faster (not for internal Temp Sense Mode)

0 = 1x conversion speed (6ms typical, R1, R0 = ‘00’, TEN = ‘0’, AREN = ‘0’)
1 = 2x conversion speed (3ms typical, R1, R0 = ‘00’, TEN = ‘0’, AREN = ‘0’)

ADCS: Start (restart) the Temp ADC (single conversion control if CEN = 0)

0 = No Start/Restart Temp ADC
1 = Start/Restart Temp ADC (each write of a ‘1’ causes single conversion; when conversion is completed ADCS = ‘0’)

ISEN: $TEMP_{IN}$ Current source (I_{TEMP}) Enable

1 = Enable 7µA current source, I_{TEMP}
0 = Disable 7µA current source, I_{TEMP}

CEN: Enable Temp ADC Continuous Conversion Mode

1 = Continuous Conversion mode
0 = Noncontinuous Conversion mode

TEN: Internal Temperature Mode Enable

1 = Enable Internal Temperature Mode
0 = External Signal Mode

For TEN = 1, set the following bits as shown:
ADC2X = 0
ADCS = set as desired
CEN = set as desired
AREN = 0
RV[1:0] = 00
M[1:0] = 00
G[1:0] = 00
R[1:0] = Set for desired Temp ADC resolution.

AREN: Temp ADC internal reference enable

1 = Enable Temp ADC internal reference (internal reference is 2.048V typical)
0 = Disable Temp ADC internal reference (use external ADC reference; see RV[1:0])

RV[1:0]: Temp ADC External Reference Select (V_{SA}, V_{EXC}, V_{REF})

M[1:0]: Temp ADC Input Mux Select

G[1:0]: Temp ADC PGA Gain Select (x1, 2, 4, or 8)

R[1:0]: Temp ADC Resolution (Conversion time) Select

Table 6-14. Temp ADC Reference Select

AREN [8]	RV1 [7]	RV0 [6]	Temp ADC Reference (V_{REFT})
0	0	0	V_{REF}
0	0	1	V_{EXC}
0	1	0	V_{SA}
0	1	1	Factory Reserved
1	X	X	Temp ADC Internal REF (2.048V)

Table 6-15. Temp ADC Input Mux Select

M1 [5]	M0 [4]	Temp ADC PGA +Input	Temp ADC PGA −Input
0	0	$TEMP_{IN}$	GND_A
0	1	V_{EXC}	$TEMP_{IN}$
1	0	V_{OUT}	GND_A
1	1	V_{REF}	$TEMP_{IN}$

Table 6-16. Temp ADC PGA Gain Select

G1 [3]	G0 [2]	Temp ADC PGA Gain
0	0	1
0	1	2
1	0	4
1	1	8

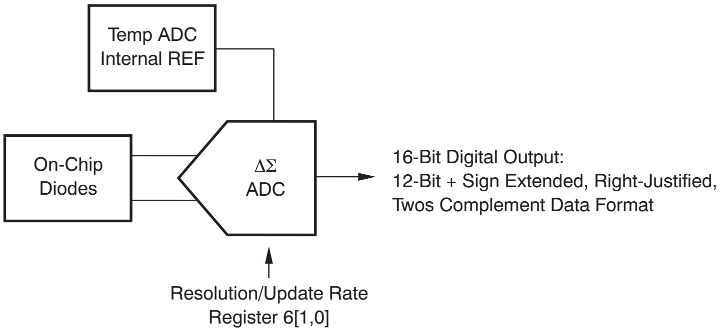


Figure 6-3. Internal Temperature Mode (Register 6 [9] = ‘1’)

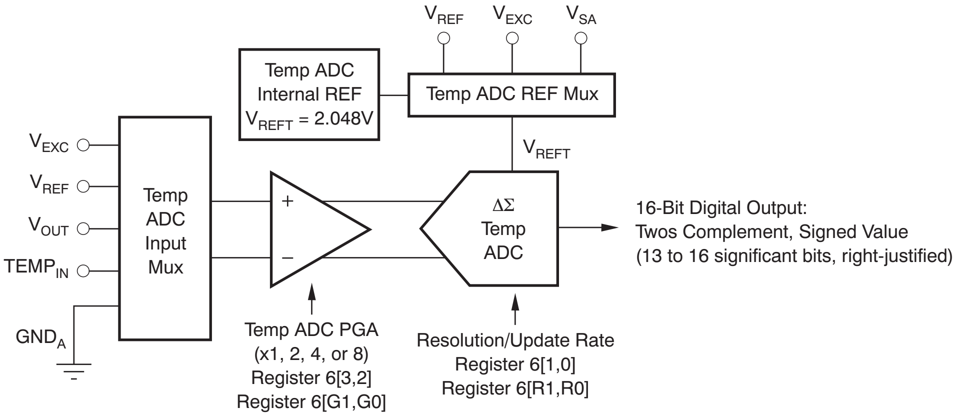
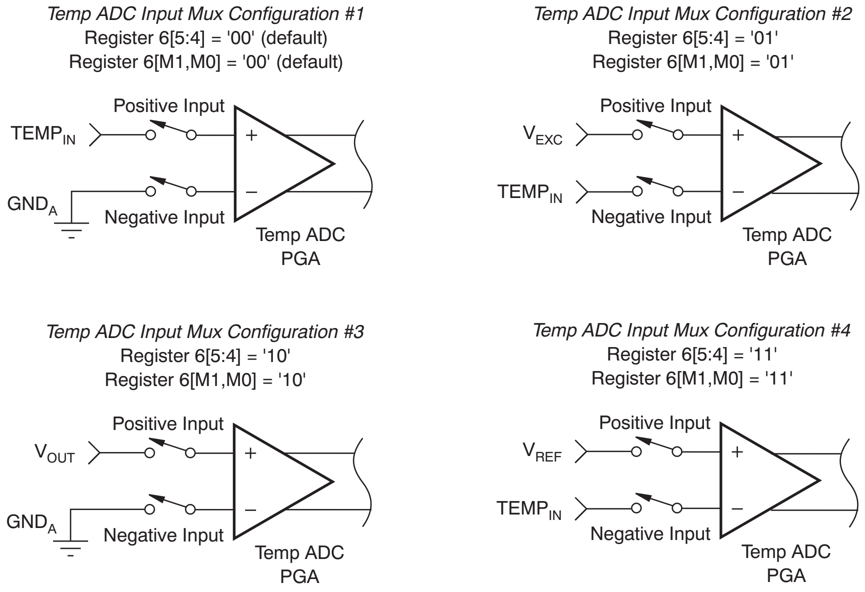


Figure 6-4. External Signal Mode (Register 6 [9], TEN = ‘0’)


Temp ADC Input Mux Configuration #1
Register 6[5:4] = '00' (default)
Register 6[M1,M0] = '00' (default)

Temp ADC Input Mux Configuration #2
Register 6[5:4] = '01'
Register 6[M1,M0] = '01'

Temp ADC Input Mux Configuration #3
Register 6[5:4] = '10'
Register 6[M1,M0] = '10'

Temp ADC Input Mux Configuration #4
Register 6[5:4] = '11'
Register 6[M1,M0] = '11'

Figure 6-5. Temp ADC Mux Configurations

Table 6-17. Temp ADC—Resolution (Conversion Time) Select

R1 [1]	R0 [0]	Internal Temperature Mode [TEN = 1]	External Signal Mode [TEN = 0], External Reference [AREN = 0]	External Signal Mode [TEN = 0], Internal Reference [2.048V, AREN = 1]
0	0	9-Bit + Sign, 0.5°C, (3ms)	11-Bit + Sign (6ms)	11-Bit + Sign (8 ms)
0	1	10-Bit + Sign, 0.25°C, (6ms)	13-Bit + Sign (24ms)	13-Bit + Sign (32ms)
1	0	11-Bit + Sign, 0.125°C, (12ms)	14-Bit + Sign (50 ms)	14-Bit + Sign (64 ms)
1	1	12-Bit + Sign, 0.0625°C, (24ms)	15-Bit + Sign (100 ms)	15-Bit + Sign (128 ms)

6.2.8 Register 7: Output Enable Counter Control Register (Read/Write, Address Pointer = 00111)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RFB	RFB	RFB	RFB	DLY3	DLY2	DLY1	DLY0	OEN7	OEN6	OEN5	OEN4	OEN3	OEN2	OEN1	OEN0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

RFB: Reserved Factory Bit: Set to zero for proper operation

DLY[3:0]: Temp ADC Delay

Temp ADC begins conversion after DLY[3:0] x 10ms after valid WRITE to this register. Initial count, DLY[3:0] is decremented every 10ms to zero count and then Temp ADC is enabled. This allows for linearization and excitation analog circuitry to settle before applying temperature compensation.

OEN[7:0]: Output Enable Counter for One-Wire Interface/V_{OUT} Multiplexed Mode.

V_{OUT} is enabled after a valid WRITE to this register. Any non-zero value = V_{OUT} Enable initial count, decremented every 10ms to zero count, and then $V_{OUT}$is disabled. After V_{OUT} is disabled, a one-second internal timer is set. If serial communication takes place from an outside controller on either the One-Wire interface (PRG pin) or Two-Wire interface, then V_{OUT} will remain disabled as long as the PGA309 is addressed at least once per second.

Table 6-18. Temp ADC—Delay After V_{OUT} Enable

DLY3 [11]	DLY2 [10]	DLY1 [9]	DLY0 [8]	Decimal Equivalent (Initial Counter Value)	Temp ADC Delay [1] (ms)
0	0	0	0	0	0
0	0	0	1	1	14
0	0	1	0	2	28
0	0	1	1	3	42
0	1	0	0	4	56
0	1	0	1	5	70
0	1	1	0	6	84
0	1	1	1	7	98
1	0	0	0	8	112
1	0	0	1	9	126
1	0	1	0	10	140
1	0	1	1	11	154
1	1	0	0	12	168
1	1	0	1	13	182
1	1	1	0	14	196
1	1	1	1	15	210

(1) Temp ADC Delay = Initial Counter Value x 14ms

Table 6-19. Output Enable Counter for One-Wire Interface/V_{OUT} Multiplexed Mode

Digital Input OEN7……OEN0 [7……0] (Binary)	Decimal Equivalent (Initial Counter Value)	V_{OUT} Enable Timeout [(1)] (ms)
0000 0000	0	0 (V_{OUT} disabled)
0010 0000	32	448
0100 0000	64	896
0110 0000	96	1344
1000 0000	128	1792
1010 0000	160	2240
1100 0000	192	2688
1110 0000	224	3136
1111 1111	255	3570

[(1)] V_{OUT} Enable Timeout = Initial Counter Value x 14ms

6.2.9 Register 8: Alarm Status Register (Read Only, Address Pointer = 01000)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	X	X	X	ALM8	ALM7	ALM6	ALM5	ALM4	ALM3	ALM2	ALM1	ALM0
POR Value	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X

Bit Descriptions:

ALM[8:0]: Fault Monitor Comparator Outputs (1 = Fault Condition)

See Section 2.8, *Fault Monitor*. ALM8 — A1SAT_HI
ALM7 — A1SAT_LO
ALM6 — A2SAT_HI
ALM5 — A2SAT_LO
ALM4 — A3_VCM
ALM3 — INN_HI
ALM2 — INN_LO
ALM1 — INP_HI
ALM0 — INP_LO

External EEPROM Example

This appendix uses an example to illustrate the mapping of PGA309 internal registers to external EEPROM register Configuration Data and Lookup Table coefficients.

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A.1 PGA309 External EEPROM Example

The PGA309 circuit configuration in Figure A-1 is used in the PGA309EVM (Evaluation Module) to check proper functionality of the PGA309. Table A-1 details the desired configuration for the PGA309. The Gain and Offset Scaling are shown in Example A-1. Figure A-2 shows how the internal PGA309 16-bit data is mapped into the external EEPROM 8-bit address locations. The external EEPROM values are displayed in Table A-2, which also details how Checksum1 and Checksum2 are computed for this example.

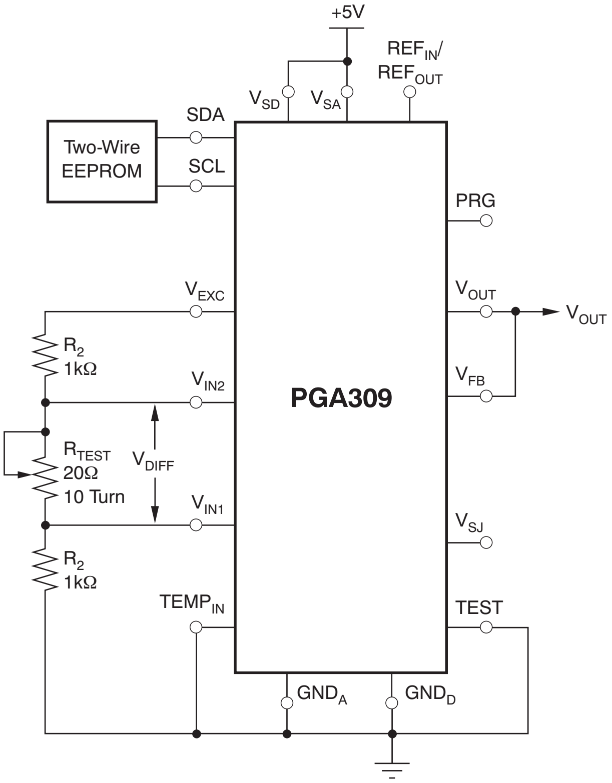

Figure A-1. PGA309 Circuit for External EEPROM Example

Table A-1. PGA309 Configuration for External EEPROM Example

Parameter	Desired Setting	Comments
V_{DIFF}	0V to 33.67mV	Adjust RTEST from 0Ω to 20Ω
V_{REF}	4.096V	Use Internal PGA309 Reference
V_{EXC}	3.4V	Use Linearization Circuit, Range 0 (K_{EXC} = 0.83), Lin DAC = 0
Coarse Offset	−3.277mV	
Front-End PGA Gain	64	
Gain DAC	1	
Output Amplifier Gain	2.4	
Zero DAC	100mV	
Over-Scale	3.876V	
Under-Scale	0.245V	
V_{OUT} Ideal	−0.263V to +4.908V	With Over-Scale and Under-Scale Disabled
V_{OUT} Final	0.245V to 3.876V	With Over-Scale and Under-Scale Enabled

Table A-1. PGA309 Configuration for External EEPROM Example (continued)

Parameter	Desired Setting	Comments
Fault Detection	External Comparators	Enable
	Fault Detect Polarity	Positive
	Internal Comparators	Disable
Temperature ADC	Internal Mode	
Output Enable Counter	Set To All Zeroes	
EEPROM Temperature Coefficients		Set so all temperatures ≤ +128°C use same Gain DAC and Zero DAC settings

Example A-1. Gain and Offset Scaling for External EEPROM

$V_{OUT} = V_{DIFF}$ (Front-End PGA Gain)(Gain DAC)(Output Amplifier Gain) + Coarse Offset (Front-End PGA Gain)(Gain DAC)(Output Amplifier Gain) + Zero DAC (Gain DAC)(Output Amplifier Gain)

$V_{OUT} = V_{DIFF}\,(64)(1)(2.4) + -3.277\text{mV}\,(64)(1)(2.4) + 100\text{mV}$

$(1)(2.4)\;V_{OUT} = V_{DIFF}\,(153.6) - 0.2633\text{V}$

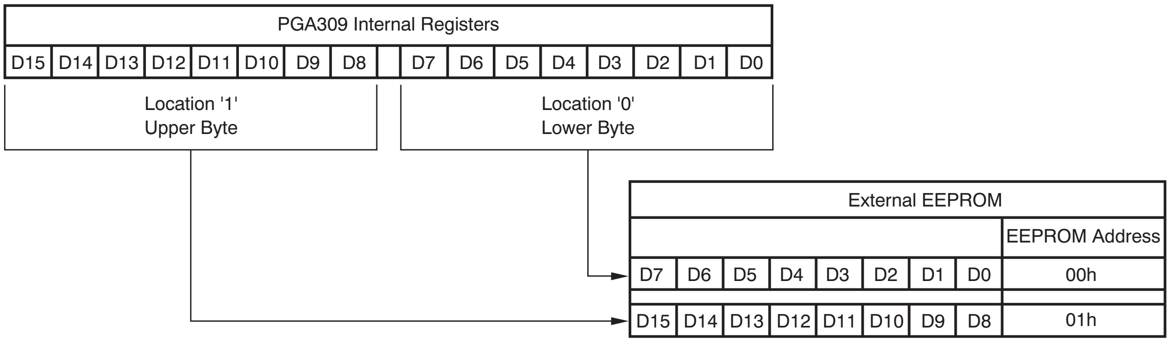

Figure A-2. Gain and Offset Scaling for External EEPROM Example

Table A-2. Final Values for External EEPROM Example

8-Bit EEPROM Load				**Location ‘1’**								**Location ‘0’**								
PGA309 External EEPROM First Part (Configuration Data)				**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	
				Upper Byte								**Lower Byte**								
External EEPROM Address (Decimal)	**PGA309 Internal Reg Address**	**PGA309 Internal Address Description**	**Data**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex Equiv**
1/0 MSB/LSB			Programmed flag value must be as shown	0	1	0	1	0	1	0	0	0	1	0	0	1	0	0	1	5449
3/2 MSB/LSB			Unused; set to zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
5/4 MSB/LSB			Unused; set to zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
7/6 MSB/LSB	00011 (Register 3)	Reference Control and Linearization		RFB	RFB	RFB	RFB	EXS	EXEN	RS	REN	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	
7/6				0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0500
9/8 MSB/LSB	00100 (Register 4)	PGA Coarse Offset and Gain/Output Amplifier Gain		OWD	GO2	GO1	GO0	GI3	GI2	GI1	GI0	RFB	RFB	RFB	OS4	OS3	OS2	OS1	OS0	
9/8				0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	1	1611
11/10 MSB/LSB	00101 (Register 5)	PGA Configuration and Over/Under Scale Limit		RFB	RFB	CLK_ CFG1	CLK_ CFG0	EXTEN	INTEN	EXTPO L	INTPOL	RFB	OU EN	HL2	HL1	HL0	LL2	LL1	LL0	
11/10				0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	0A47
13/12 MSB/LSB	00110 (Register 6)	Temperature ADC Control		RFB	RFB	ADC2X	ADCS	ISEN	CEN	TEN	AREN	RV1	RV0	M1	M0	G1	G0	R1	R0	
13/12				0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1603
																				SUM = 8FA4h

Table A-2. Final Values for External EEPROM Example (continued)

8-Bit EEPROM Load				**Location '1'**								**Location '0'**								
PGA309 External EEPROM First Part (Configuration Data)				**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	
				Upper Byte								**Lower Byte**								
External EEPROM Address (Decimal)	**PGA309 Internal Reg Address**	**PGA309 Internal Address Description**	**Data**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex Equiv**
15/14 MSB/LSB		FFFF – sum(hex equiv of each location – 1/10 through 13/12) truncated above 16 bits	Checksum1	1	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	705B
17/16 MSB/LSB			T0 (Temp Index value for Temp ≤ T0)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0800
19/18 MSB/LSB			Z0 (Zero DAC value for Temp ≤ T0)	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0640
21/20 MSB/LSB			G0 (Gain DAC value for Temp ≤ T0)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
23/22 MSB/LSB			T_{END} (end of Lookup Table)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7FFF
25/24 MSB/LSB			ZM_{END} (end of Lookup Table)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
																				SUM = 18E3Eh
27/26 MSB/LSB		FFFF – sum(hex equiv of each location – 17/16 through 25/24) truncated above 16 bits	GM_{END} (Checksum2)	1	0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	71C1

Detailed Block Diagram

Appendix B shows a detailed block diagram of the PGA309.

Topic **Page**

B.1 Detailed Block Diagram

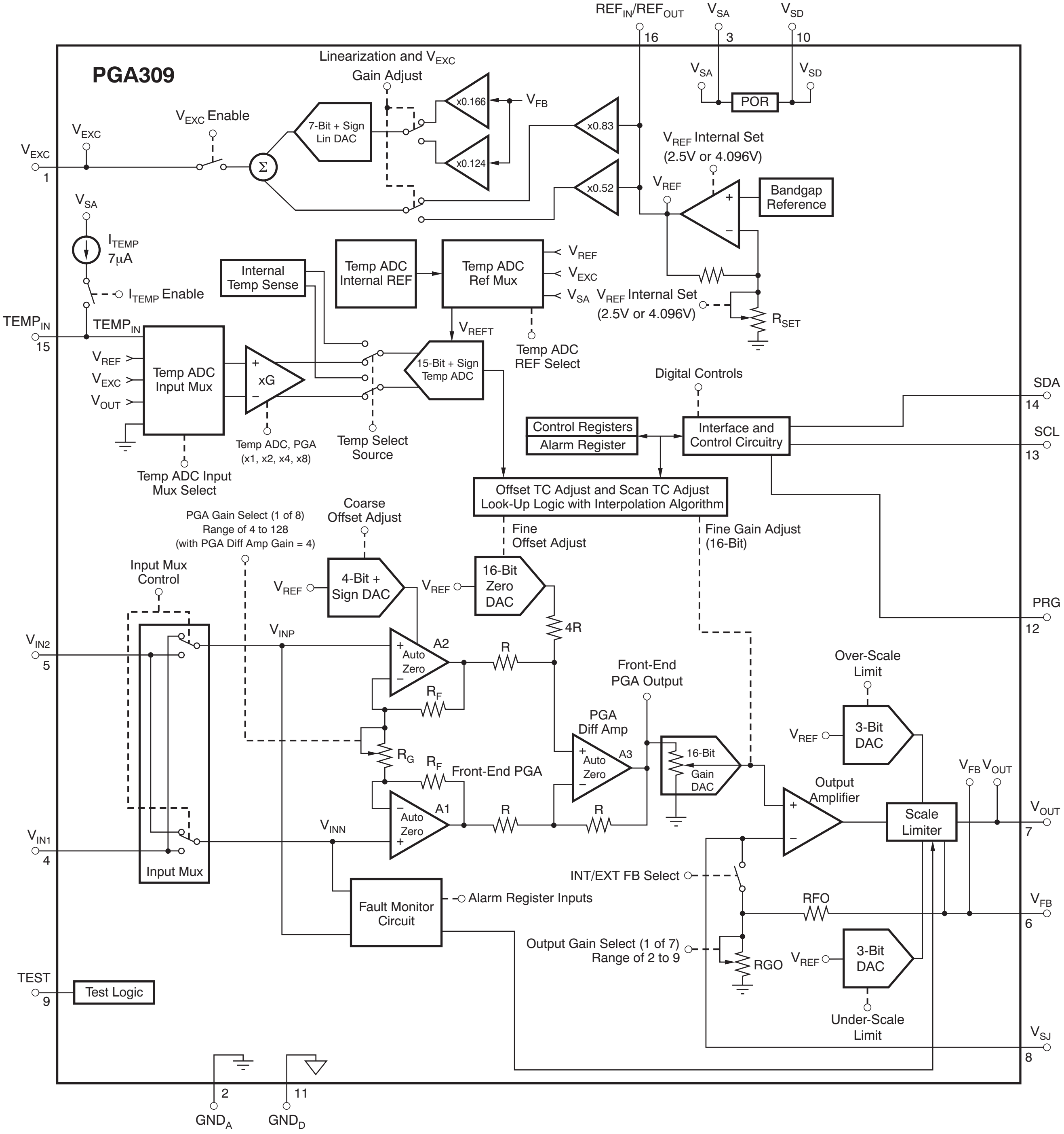

Figure B-1. Detailed Block Diagram

Appendix C

Glossary

A

ADC— Analog-to-digital converter

B

B_V— Bridge nonlinearity with applied pressure.

$$B_V = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{\left(\frac{4 \bullet V_{REF} \bullet K_{EXC}}{K_{LIN}}\right) + 4 \bullet (V_{OUT\_MAX} + V_{OUT\_MIN})}$$

$B_{V\ MAX}$—Maximum compensable nonlinearity

$B_{V\ -MAX}$—

$$B_{V\ -MAX} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{\left(\frac{4 \bullet V_{REF} \bullet K_{EXC}}{K_{LIN\ -MAX}}\right) + 4 \bullet (V_{OUT\_MAX} + V_{OUT\_MIN})}$$

$B_{V\ +MAX}$—

$$B_{V\ +MAX} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{\left(\frac{4 \bullet V_{REF} \bullet K_{EXC}}{K_{LIN\ +MAX}}\right) + 4 \bullet (V_{OUT\_MAX} + V_{OUT\_MIN})}$$

C

C_F— External feedback capacitor connected between V_{SJ} and V_{OUT}, for stability.

CMR— Common-mode rejection

D

DAC— Digital-to-analog converter

E

EMI— Electromagnetic interference

F

FSR— Full-scale range of PGA309 output.

$$FSR = V_{OUT\_MAX} - V_{OUT\_MIN}$$

FSS— Full-scale bridge sensitivity for sensor at P_{MAX} (for example, 2mV/V).

G

G_{IDEAL}— Ideal gain

$$G_{IDEAL} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{REF} \bullet FSS}$$

G_L— Gain of the PGA309 when using the Linearization circuit.

$$G_L = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{REF} \bullet K_{EXC} \bullet FSS) + (K_{LIN} \bullet V_{OUT\_MAX} \bullet FSS)}$$

GND_A— Analog ground

GND_D— Digital ground

G_T— Total gain produced by the PGA309 of V_{OUT}/V_{IN} gain.
G_T = (Front-End PGA Gain)(Gain DAC)(Output Amplifier Gain)

I

IVR— Input voltage range of the PGA309.

K

K_{LIN}— PGA linearization coefficient

$$K_{LIN} = \frac{4 \bullet B_V \bullet V_{REF} \bullet K_{EXC}}{(V_{OUT\_MAX} - V_{OUT\_MIN}) - 2 \bullet B_V \bullet (V_{OUT\_MAX} + V_{OUT\_MIN})}$$

$K_{LIN\ -MAX}$—Most negative linearization coefficient. Its value is determined by the selected range of bridge sensor nonlinearity compensation.

$K_{LIN\ +MAX}$—Most positive linearization coefficient. Its value is determined by the selected range of bridge sensor nonlinearity compensation.

K_{EXC}— PGA excitation coefficient. Scale factor on V_{REF}.

K_P— Pressure constant. Converts linear input pressure to nonlinear pressure detected by sensor; referenced to full-scale input pressure.

L

LSB— Least significant bit

M

MSB— Most significant bit

P

P— Pressure input

P_{MIN}— Minimum sensor input pressure

P_{MAX}— Maximum sensor input pressure

PNL— Nonlinear pressure output of bridge with linear pressure input P.

POR— Power-on reset function

PRG— Single-wire interface program pin

R

R_{BRG}— Bridge resistor value

R_{FB}— External feedback resistor connected to V_{FB}.

R_{FO}— Internal feedback resistor for the Output Amplifier.

$R_{FO\ EXT}$—Additional external feedback resistor for the Output Amplifier.

R_{GO}— Internal gain resistor for the Output Amplifier.

$R_{GO\ EXT}$—Additional external gain resistor for the Output Amplifier.

R_{ISO}— External isolation resistor connected to V_{OUT}.

REF_{IN}/REF_{OUT}— Voltage reference input/output pin

RFI— Radio frequency interference

RTO— Referred-to-output

S

SCL— Clock input/output for Two-Wire serial interface

SDA— Data input/output for Two-Wire serial interface

T

$TEMP_{IN}$— External temperature signal input

TEST— Test/external controller mode pin

V

V_{BRMAX}— Maximum bridge sensor output

V_{CM}— Common-mode voltage applied to the PGA309 input.

$$V_{CM} = \left(\frac{V_{INP} + V_{INN}}{2}\right)$$

V_{COS}— Coarse offset voltage output of the coarse offset adjust DAC.

V_{DIFF}— Differential voltage applied to the PGA309 inputs.
$V_{DIFF} = V_{INP} - V_{INN}$

V_{EXC}— Bridge sensor excitation voltage

$$V_{EXC} = V_{REF} \bullet K_{EXC} + K_{LIN} \bullet V_{OUT}$$

$V_{EXC\ MAX}$—Maximum bridge sensor excitation voltage

$$V_{EXC\ MAX} = V_{REF} \bullet K_{EXC} + K_{LIN} \bullet V_{OUT\_MAX}$$

$V_{EXC\ MIN}$—Minimum bridge sensor excitation voltage

$$V_{EXC\ MIN} = V_{REF} \bullet K_{EXC} + K_{LIN} \bullet V_{OUT\_MIN}$$

$\mathbf{V_{FB}}$— V_{OUT} feedback pin

$\mathbf{V_{FRONT}}$— The output of difference amplifier A3, of the Front-End PGA309.

$\mathbf{V_{IN1}}$— Signal input voltage 1

$\mathbf{V_{IN2}}$— Signal input voltage 2

$\mathbf{V_{INN}}$— The positive input of internal auto-zero amplifier A1, of the Front-End PGA.

$\mathbf{V_{INP}}$— The positive input of internal auto-zero amplifier A2, of the Front-End PGA.

$\mathbf{V_{N}}$— Output voltage of one branch of the bridge.

$\mathbf{V_{OA1}}$— Output voltage of internal auto-zero amplifier A1.

$$V_{OA1} = V_{CM} - G\left(\frac{V_{DIFF}}{2}\right)$$

$\mathbf{V_{OA2}}$— Output voltage of internal auto-zero amplifier A2.

$$V_{OA2} = V_{CM} + G\left(\frac{V_{DIFF}}{2}\right)$$

$\mathbf{V_{OS}}$— Sensor offset voltage

$\mathbf{V_{OUT}}$— Analog output voltage of conditioned sensor

$\mathbf{V_{OUT\ ERR\ FSR}}$—Error in %FSR of V_{OUT}

$\mathbf{V_{OUT\ FILT}}$—Filtered V_{OUT}

$\mathbf{V_{OUT\ IDEAL}}$—Ideal output for a given pressure, P.

$$V_{OUT\_IDEAL} = FSS \bullet G_{IDEAL}\left(\frac{P}{P_{MAX}}\right)V_{REF} + V_{OS}$$

$\mathbf{V_{OUT\ MAX}}$—V_{OUT} for maximum bridge sensor output

$\mathbf{V_{OUT\ MIN}}$—V_{OUT} for minimum bridge sensor output

$\mathbf{V_{P}}$— Output voltage of one branch of the bridge.

$\mathbf{V_{REF}}$— Reference voltage used by the PGA309 (internal or external).

$\mathbf{V_{REFT}}$— Temperature V_{REF}

$\mathbf{V_{S}}$— Supply voltage

$\mathbf{V_{SA}}$— Analog supply voltage

$\mathbf{V_{SD}}$— Digital supply voltage

$\mathbf{V_{SJ}}$— Output Amplifier summing junction

$\mathbf{V_{TEST}}$— Test signal

$\mathbf{V_{ZERO\ DAC}}$—Output voltage of the Zero DAC

Revision History

Changes from A Revision (January, 2005) to B Revision **Page**

- Updated document format to current standards 1
- Added Table 2-4 7
- Changed Table 2-5 7
- Updated Table 6-8 8
- Added Table 6-9 8
- Changed times indicated in *Power-Up and Normal Operation* section 15
- Added note to Figure 2-1 20
- Revised Figure 2-3 and added note 22
- Added *PGA Transfer Function* section 22
- Added Table 2-4 36
- Changed Table 2-5 37
- Changed time values for power-on reset timeout discussed in Section 2.7.1 42
- Corrected time values indicated for wait times 60
- Revised Figure 3-1 61
- Changed wait time indicated for Checksum Error event 70
- Revised Figure 4-7 79
- Changed Figure 4-8 80
- Updated Section 4.9; changed indicated time values, Figure 4-13, and Figure 4-14 86
- Revised Section 4.11; added Figure 4-18 through Figure 4-21 91
- Updated Table 6-8 109
- Added Table 6-9 110
- Corrected typos in Table 6-17 115
- Updated *Temp ADC Delay* column values and footnote (1) in Table 6-18 116
- Corrected V_{OUT} *Enable Timeout* column values and footnote (1) in Table 6-18 117
- Corrected typo in Figure B-1 126

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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