Stroke Rehabilitation Hand Device (Checkpoint)

TEAM #15
MEMBERS: JAKE CARDUCCI, KEVIN OLDS (MENTOR)

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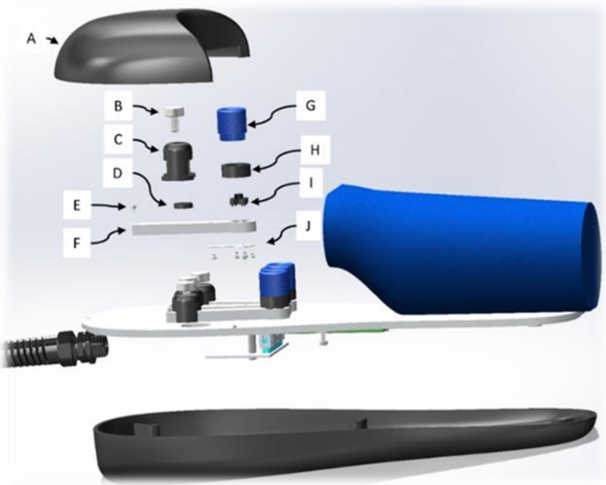
Planned Goal

To get clinical engineering approval and an IRB-approved clinical study for a hand rehabilitation device, to design and fabricate an improved version of the device based on study feedback, and to get preliminary study feedback for the revised version.

Technical Summary (Current Prototype)

- Hand fits in adjustable brace, secures to base
- Finger fits in silicon cup(s), force detected at base
- Force signals sent to computer and processed into usable information



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Technical Approach (Planned Prototype)

- Increase digit count from two to five
  - 8 → 20 signal channels
- Modify mechanisms for easier component attachment and removal (brace, retention cups, etc.)
- Properly calibrate force sensors with high sensitivity
- Modified adjustable force beam designs for each finger

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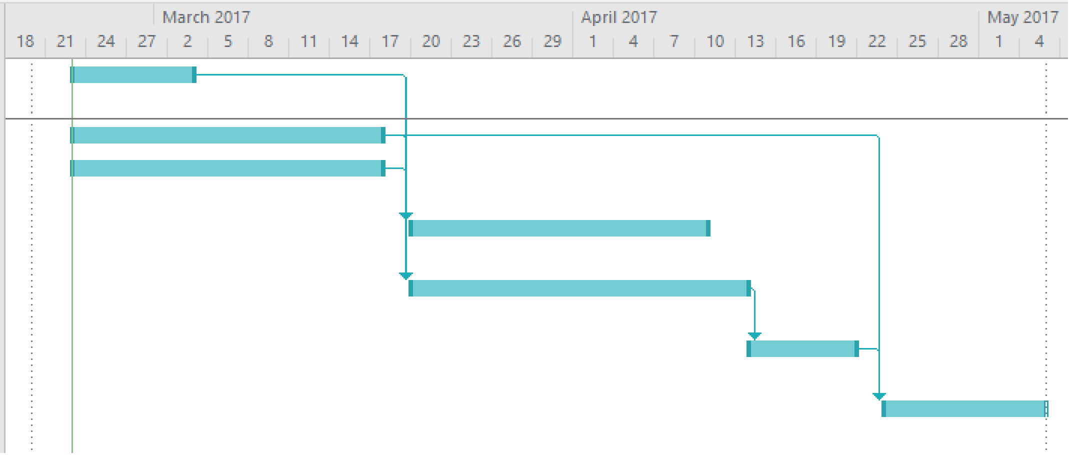
Original Schedule

Task Name	Duration	Start	Finish	Predecesso
CES Approval Stamp for Original Prototype	7 days	Thu 2/23/17	Fri 3/3/17	
IRB Approval	17 days	Thu 2/23/17	Fri 3/17/17	
Design Revisional Prototype	17 days	Thu 2/23/17	Fri 3/17/17	
Get Patient Feedback for Original Prototype	16 days	Mon 3/20/17	Mon 4/10/17	2,1
Fabricate Revisional Prototype	19 days	Mon 3/20/17	Thu 4/13/17	3
CES Approval Stamp for Revisional Prototype	6 days	Fri 4/14/17	Fri 4/21/17	5
Get Patient Feedback for Revisional Prototype	10 days	Mon 4/24/17	Fri 5/5/17	6,2



IRB / CES Update

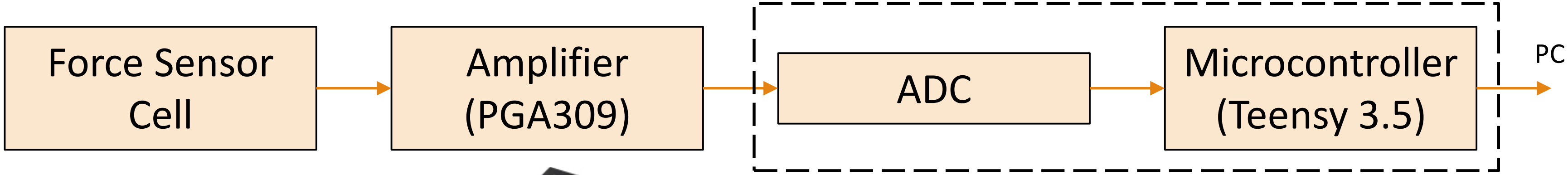
- Compliance Training
  - Human subjects research (CITI)
  - HIPAA for research
- Clinical engineering a
  - Wrote select
  - Ex: 3

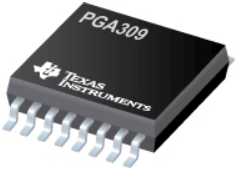
No first prototype testing

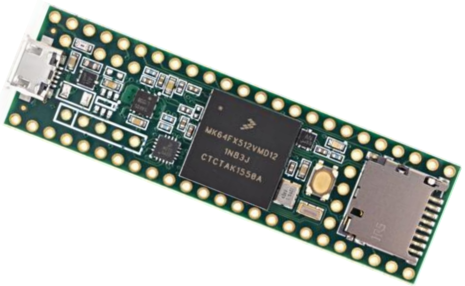
IRB / CES Update

- Western University collaboration
  - Device validation study
  - Funded through CA grant
  - Targeted at clinics across Canada
  - 3-4 devices ready by mid-May
- **Therefore, planned / completed tasks related to IRB and CES approval are on hold until further notice**

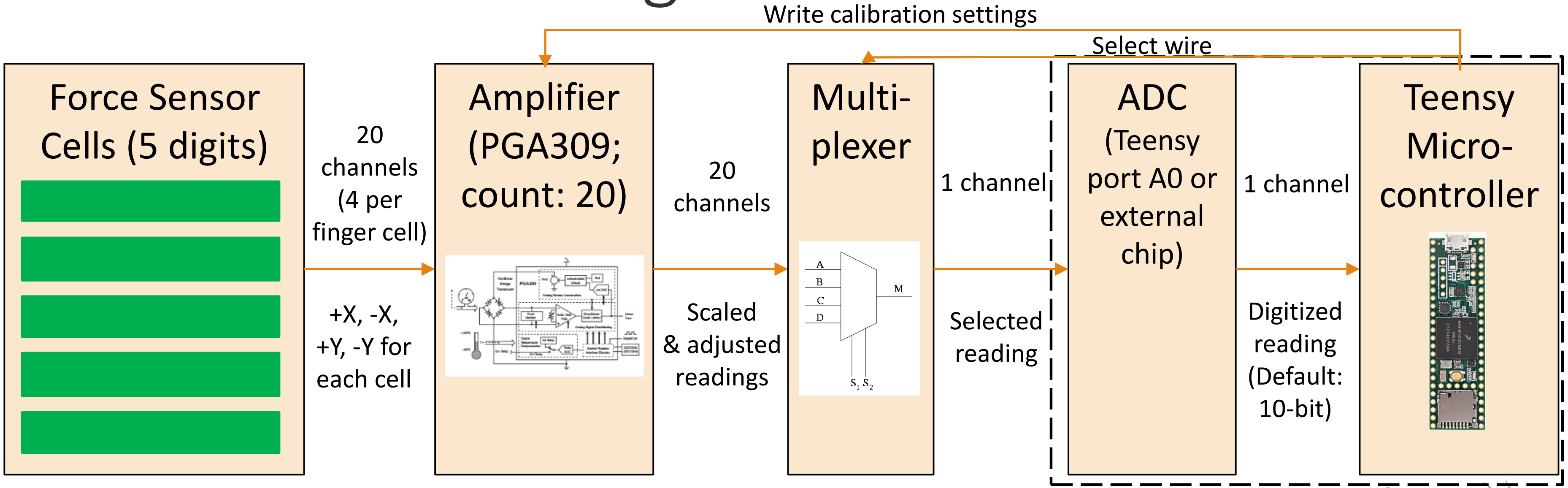
DAQ Channel Design







DAQ Channel Design

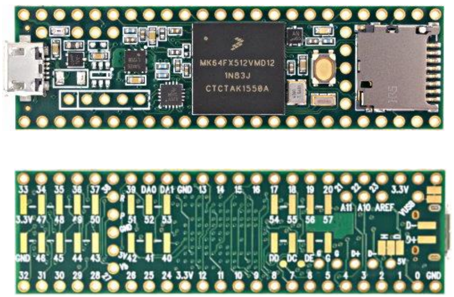


+Z, -Z can be found from +X, -X, +Y, -Y

DAQ Channel Design

- PGA309 Amplifier
  - Programmable gain controller
  - 0.25 in x 0.20 in x 0.05 in*
  - Potential gain range: 2.7V/V to 1152 V/V
  - Digital calibration over I^2C communication
  - Internal fault detection
  - Temperature-based offset adjustment

- Teensy 3.5 USB Microcontroller
  - 32-bit width, 120 MHz clock, 192 KB RAM
  - Very small footprint (2.4 by 0.7 inches)*
  - Programmable via Arduino IDE
  - 2 to 12 MHz built-in ADC sampling rate (all bit resolutions)



*(By comparison, NI DAQ board: 3.9 in x 2.5in x 12 mm)

DAQ Channel Design

- 3-stage gain amplifier
  - Front-End PGA (GI = 4 to 128)
  - Fine DAC (GD = 0.33 to 1)
  - Output Amp (GO = 2 to 9)
- Transfer Function
  - $V_{out} = \left[\left(sign_{mux} * V_{in,diff} + \mathrm{V}_{\mathrm{offset,coarse}}\right) * GI + V_{zero,DAC}\right] * GD * GO$
  - Except for input voltage and multiplex sign, you can program each one of these!

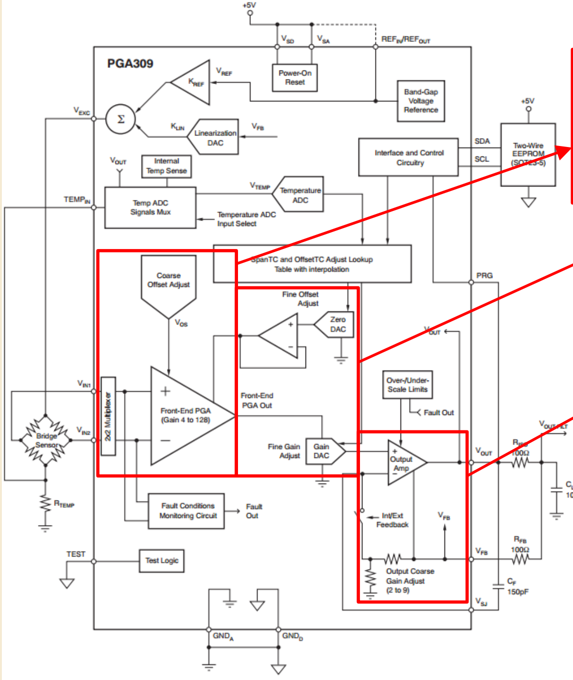


Figure 24. Simplified Diagram of the PGA309 in a Typical Configuration

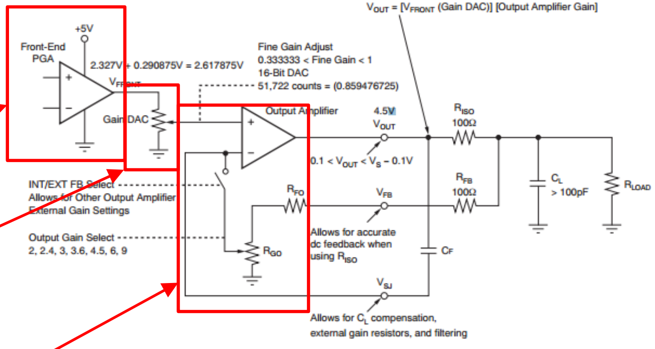
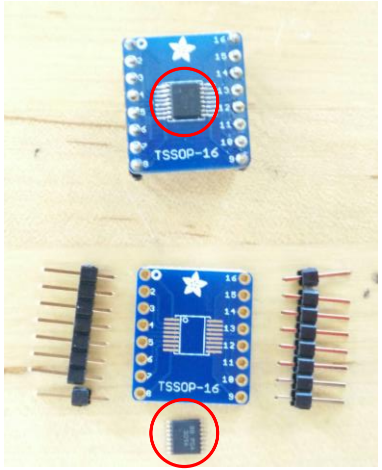
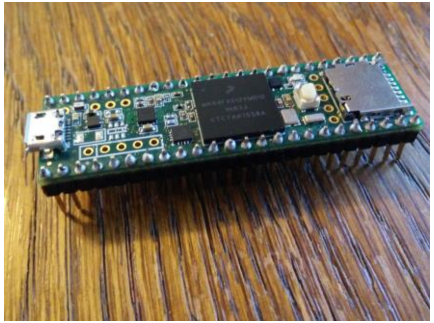


Figure 2-3. Fine Gain Adjust of the PGA309

DAQ Channel Design

- Amplifier verification testing
  - Needed early in design
- Soldering
  - TSSOP-16 breakout adapter (0.65 mm pin separation)
  - Breadboard headers (2.54 mm pin separation)
  - Former required more care and caution than the latter





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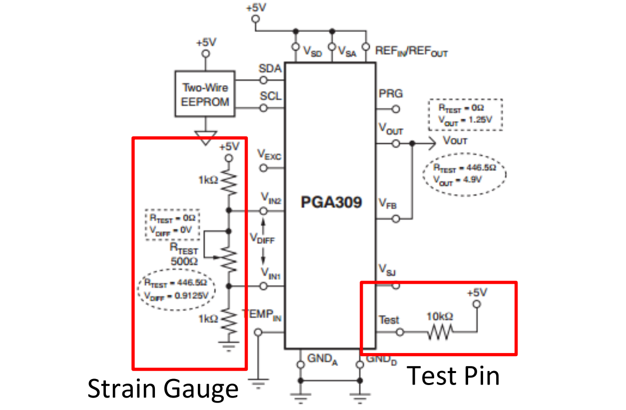
DAQ Channel Design

- Q: How to know if amplification on the PGA309 is working?
- A: Use the test pin configuration.
- How?: Bring test port (pin 9) to HIGH
- Result: V_{out} enabled & default gain/offset values used

Table 3-8. POR States for Key Parameters

Parameter	POR State
Coarse Offset	0V
Front-End PGA Gain	4 ($V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$)
Gain DAC	0.5
Output Amplifier Gain	2
Zero DAC	$0.25V_{REF}$
V_{REF} Select	External Reference
Lin DAC	0
Fault Monitor	Disabled
Over/Under-Scale	Disabled
V_{EXC}	Disabled
I_{TEMP}	Disabled
Temp ADC	External Signal Mode



NOTE: Two conditions for V_{DIFF} and the resulting V_{OUT} are shown in this figure. Condition one is in a dashed, square box. Condition two is shown in a dashed oval.

Figure 3-5. Signal Path Functional Check with Test = '1' on Power-Up

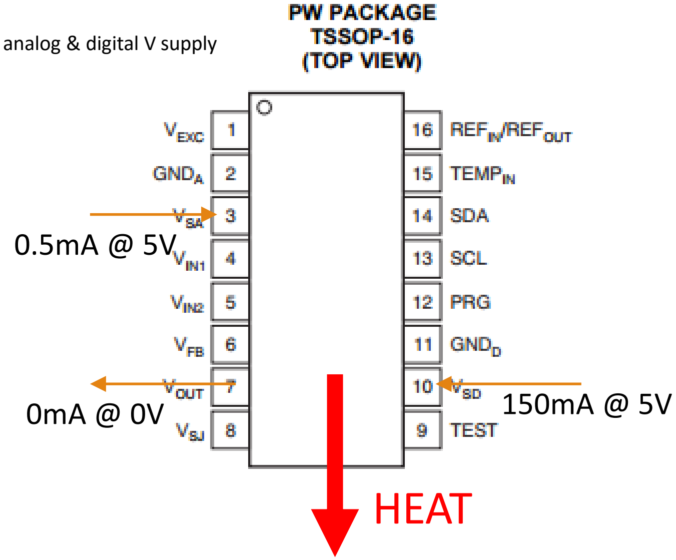
$$V_{out} = \left[\left(sign_{mux} * V_{in,diff} + \mathrm{V}_{\mathrm{offset,coarse}}\right) * GI + V_{zero,DAC}\right] * GD * GO$$

$$V_{out} = \left[\left(sign_{mux} * V_{in,diff} + 0\right) * 4 + 0.25 * V_{ref}\right] * 0.5 * 2$$

$$V_{out} = abs\left(V_{in,diff}\right) * 4 + 0.25 * V_{ref}$$

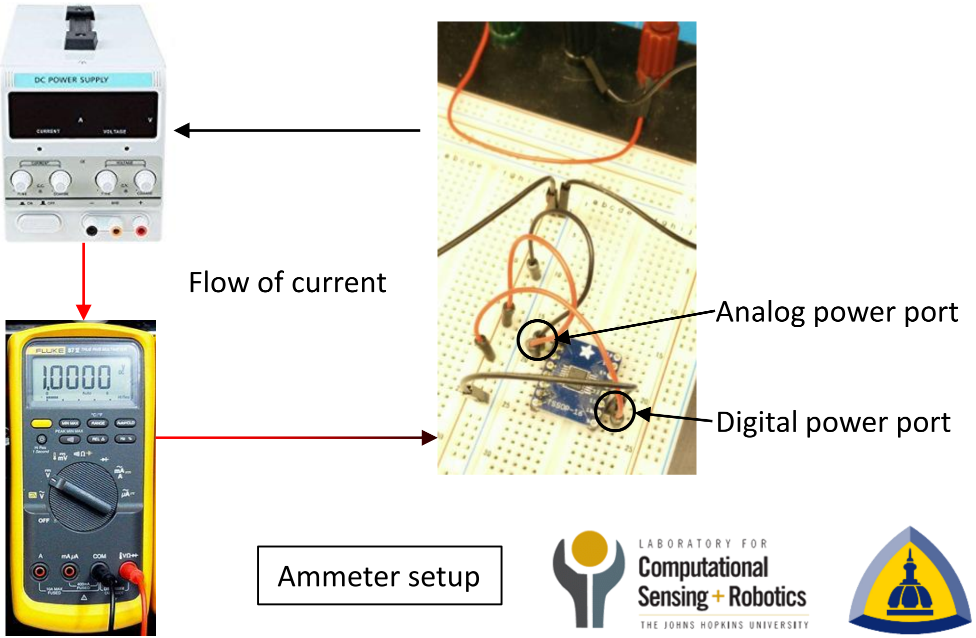
DAQ Channel Design

- Connected PGA power to Teensy USB power
- Result?
  - Chip temp increased rapidly!
  - $I_{analog} \approx 0.5$ mA into pin 3
  - $I_{digital} \approx 150$ mA into pin 10
  - Neither pin should exceed 10 mA
  - Something went wrong!



DAQ Channel Design

- Solution process
  - Isolate power connections; disconnect other connections
  - Use controlled DC lab power supply direct to PGA309
  - Chip only heated from connection hot-swaps
    - Difference in supply voltages > 200 mV
- Final solution
  - Avoid hot-swaps
- Result?
  - Chip never heats from DC supply or standalone charger



Ammeter setup

Lesson #1

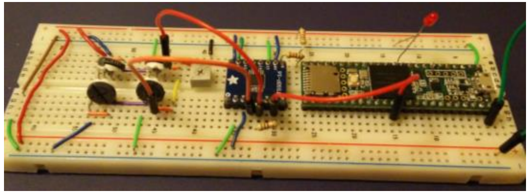
Never rush your debugging and validation processes.

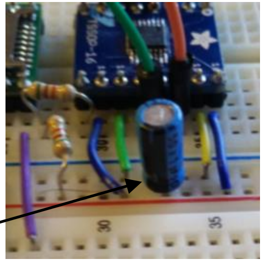
Be mindful of what and when you connect and disconnect components.

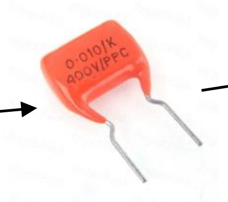
(i.e. don’t hotswap your power connections when two of them should be nearly the same <u>at all times</u>; turn off total power at the source if you need to modify connections)

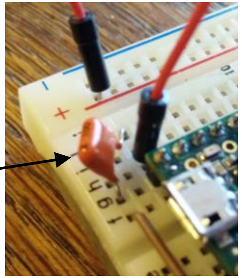
DAQ Channel Design

- Problem: chip still heated unpredictably from USB power
- Theory: Inconsistent supply from USB, leading to exceeding 200 mV supply diff
- Possible solution: add decoupling capacitors between power & ground rails
  - 1 µF near chip: charge reservoir to smooth voltage
  - 0.01 µF near power source: reduce noise from supply
- Result?:
  - Chip has not overheated since









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Lesson #2

It is rarely a bad idea to use decoupling capacitors in electronics design, even for circuits with DC power.

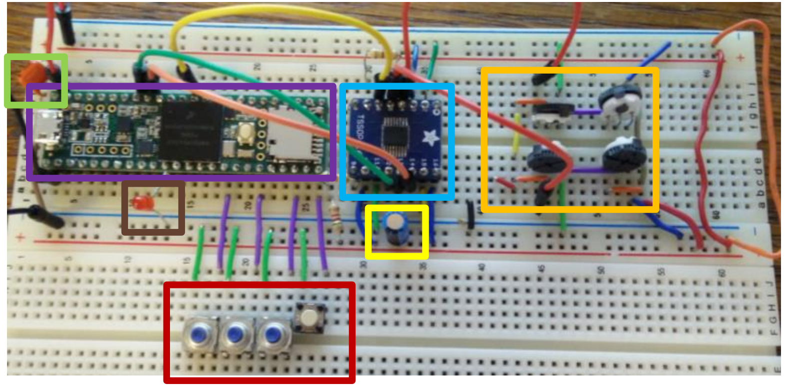
So use them whenever possible.

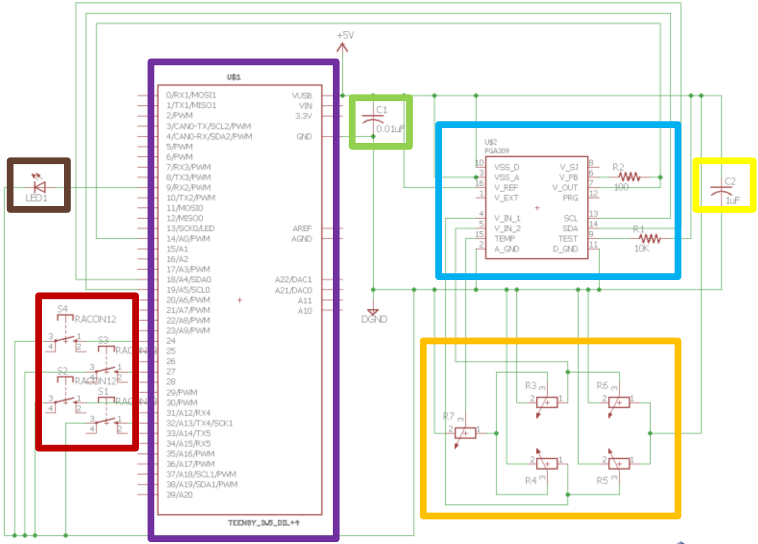
Lesson #2.5

Debugging electronic designs can be particularly frustrating, much like finding a needle in a prairie field.

DAQ Channel Design

Final calibration setup





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DAQ Channel Design

$V_{in, 1}$	$V_{in, 2}$	$V_{out, meas}$	$V_{out, calc}$	Error
2.140	1.653	3.257	3.245	0.370%
1.355	0.682	4.000	3.989	0.276%
0.989	0.435	3.515	3.513	0.057%

Test Configuration Readings (V_{ref} = 5.186 V)
$V_{out, calc}$ found from Power-on Reset TF

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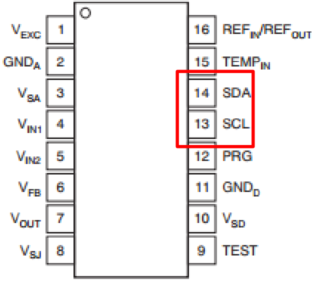
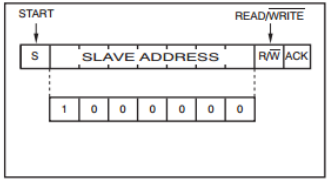
DAQ Channel Design

- Q: How do we modify gain and offset parameters?
- A: I^{2}C
  - Two-wire communication protocol
  - Data on SDA line (pin 14)
  - Clock on SCL line (pin 13)
- PGA309 designed for EEPROM chips
  - Why not just use the Teensy as a master?
  - Make PGA a slave device





PGA309 Control Byte Allocation

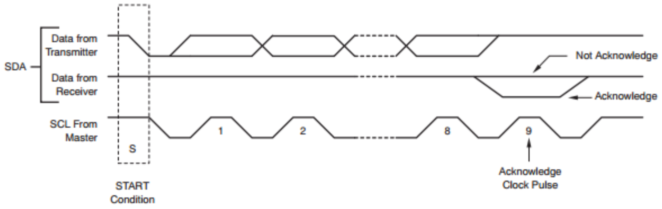


Figure 4-2. Two-Wire Start and Acknowledge

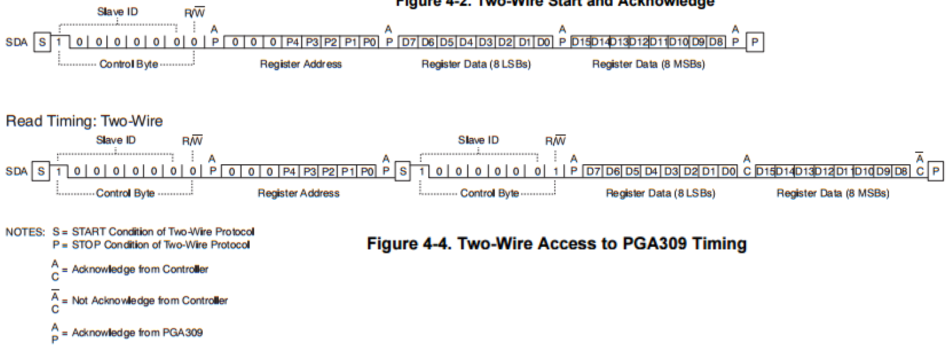
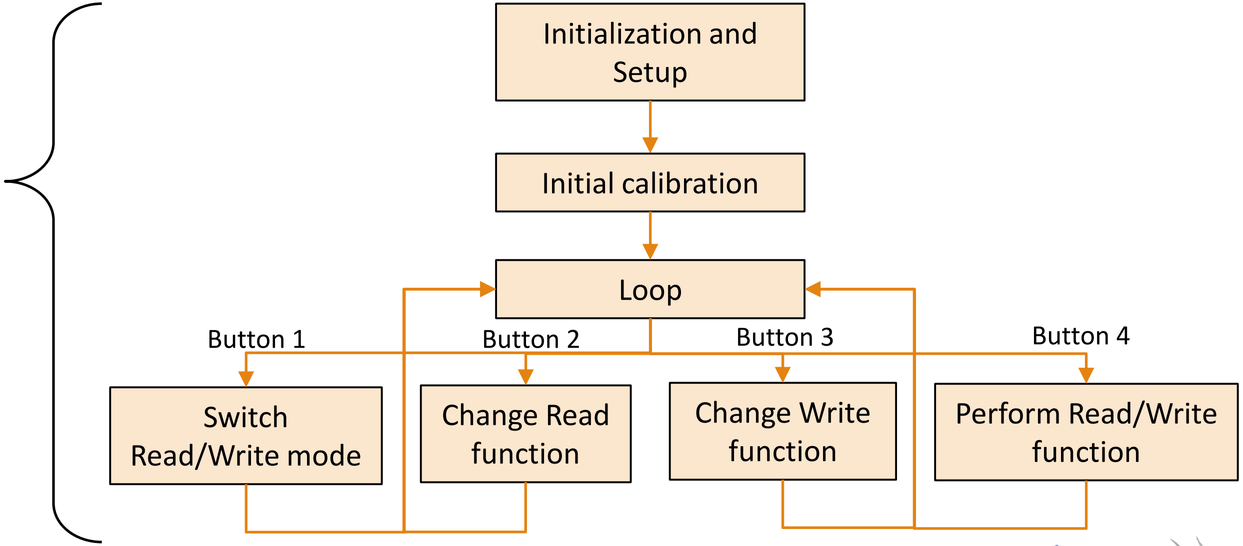


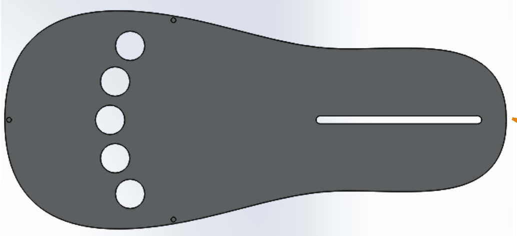
Figure 4-4. Two-Wire Access to PGA309 Timing

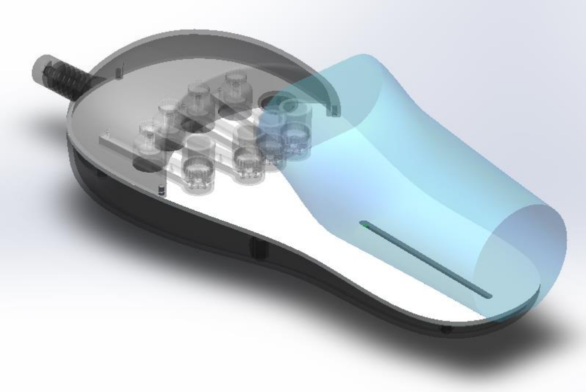
DAQ Channel Design

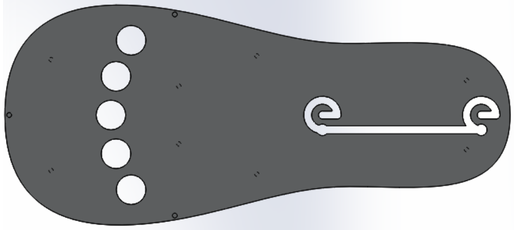
- Current progress & plan
  - PGA309-to-Teensy I^2C Arduino library
    - General flow of functions on right
    - Code available on project site
  - ADC selection
    - High sampling rate desired
    - Teensy can provide at least 102.8 kHz / channel
    - External hardware packages
  - Filter design
    - Passive low-pass
    - Reduce noise while amplifying signal → increase SNR
  - Fabricate PCB in Eagle

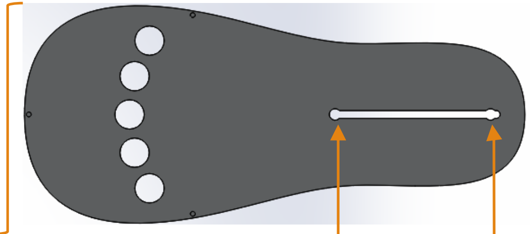


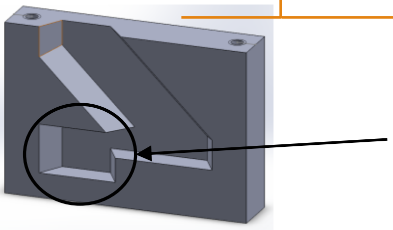
Arm Brace Attachment Design



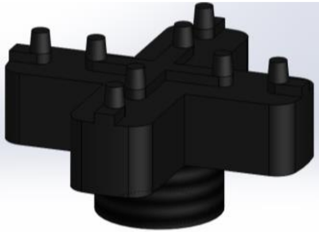


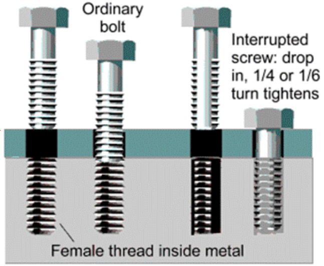


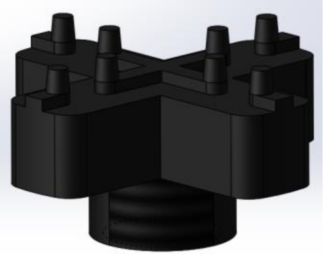


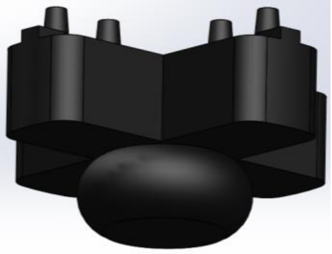


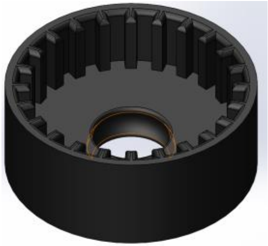
Base Cap Attachment Design

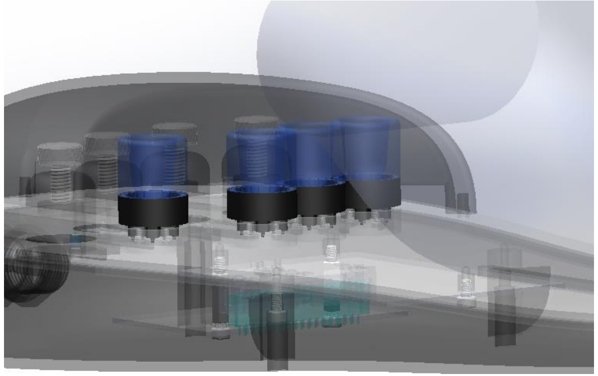




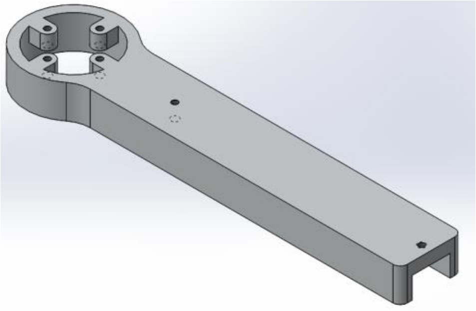


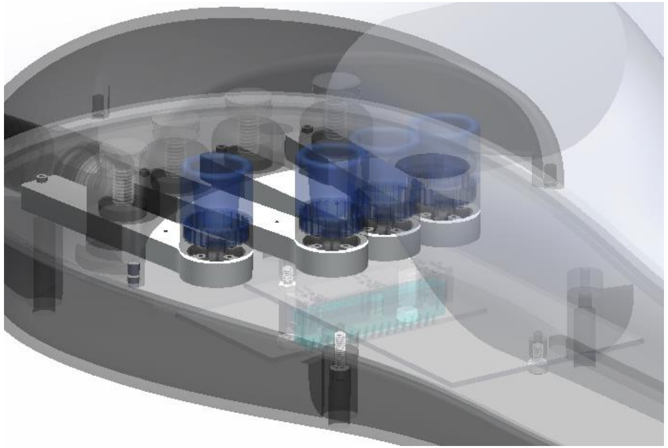


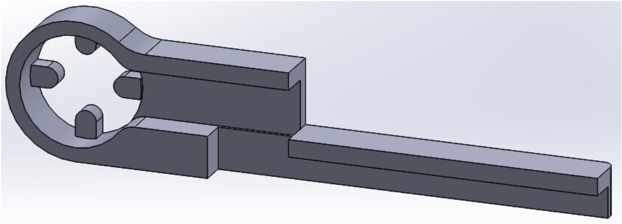




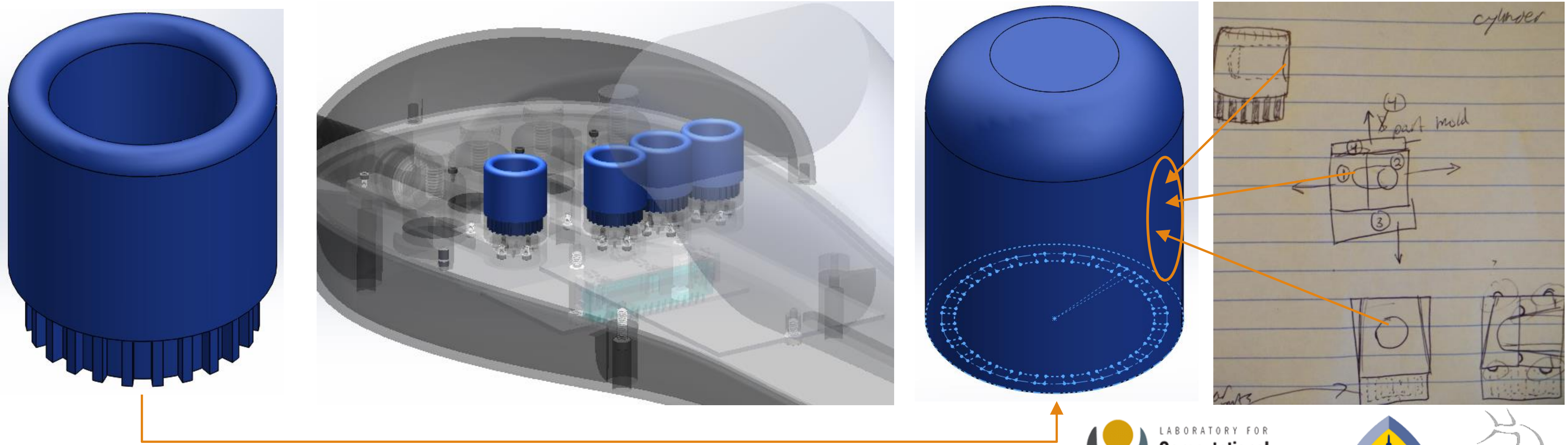
Thumb Retention Cap Design







Thumb Retention Cap Design



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Lesson #3

Make sure you clear out any ambiguities when defining project specifications or requirements as early as you can.

(i.e. a violation of an assumption regarding a project specification may lead to wasted creative energy, time, and resources typically)

Lesson #3.5 or #4

Be careful when reverse-engineering SolidWorks part models with constraint geometry established, lest you induce its wrath.

Warning	Sketch2	Could not find face or plane.
Error	Cut-Extrude1	Operation failed due to geometric condition.

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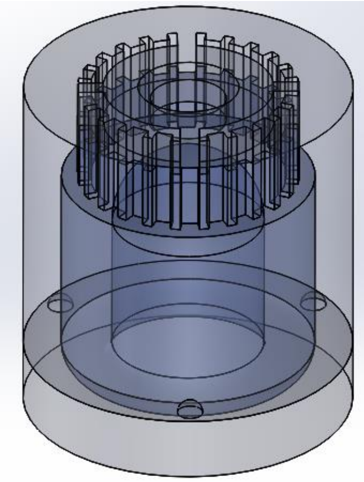
Part Fabrication and Modeling

- Current progress & plan
  - Finish CAD model for thumb retention cap
  - Evaluate alternative designs
- Fabrication
  - Aluminum machining
  - Nylon 3D printing
    - Use ProtoLabs service (1-day)
    - In-house machine shop
  - Silicone mold
    - In-house vacuum chamber
    - Plentiful silicone on hand



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Current Goal

To design a hand rehabilitation device based on technical goals and client needs, to fabricate two models of the revised design, and to get preliminary study feedback for the revised version (if possible).

Tasks and Deliverables

Minimum Tasks	Planned Date	Expected Date	Associated Deliverable
~~Send the existing prototype to clinical engineering team at JH Hospital; get approval stamp~~	~~03/03/2017~~	N/a	~~Correspondence and approval documents~~
~~Get IRB approval for a clinical study~~	~~03/17/2017~~	N/a	~~Correspondence and approval documents~~
Design a revised prototype on paper and in CAD • Easily removable arm brace • Appropriate design for thumb force sensor • Snap-on mechanism for finger retention cup adapter • PCBs for microcontroller and signal processing to support 5 fingers	03/17/2017	04/03/2017	Schematics and diagrams associated with each subsystem
~~Get feedback from at least 5 individuals affected by stroke of various degrees~~	~~04/07/2017~~	N/a	~~Force test results~~

Tasks and Deliverables

Expected Deliverables and Tasks	Planned Date	Expected Date	Associated Deliverable
Fabricate two devices from revised prototype to implement features developed from ~~patient feedback and other considerations~~ technical objectives and client needs • All designed components from revision design • Breadboard testing of components / soldering PCB parts	04/14/2017	04/28/2017	Assembled and functional revised prototypes
Maximum Deliverables and Tasks			
Send one revised prototype to clinical engineering, get approval stamp	04/21/2017	05/08/2017	Correspondence and approval documents
Get IRB approval for the clinical study	05/15/2017	05/15/2017	Correspondence and approval documents
Get feedback from at least 5 stroke-affected patients	05/05/2017	Mid-Late 2017	Force test results

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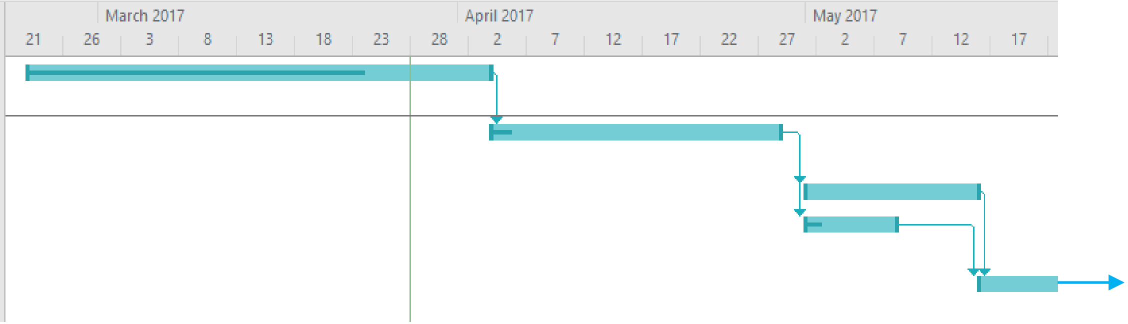
Dependencies

Dependency	Status	Resolve Plan and/or Actions Taken
Hardware from outside vendors (PCBs, printed/machined parts)	Resolved (Completed Date: 03/20/2017)	All parts needed for current design have already been acquired. Any fabrication that needs to be done can either be performed through a third party like ProtoLabs or in-house at a Hopkins-affiliated machine shop.
CES and IRB approval	'Unresolved' (Estimated Resolve Date: 05/05/2017)	If intractable delays in CES and IRB approval come up (unlikely since similar projects and devices from the same group have been approved in the past), the project will shift to focus more on technical development of the new prototype (which it has).
Patient recruiting	Unresolved (Estimated Resolve Date: 05/30/2017)	Even with CES and IRB approval, there can be delays in recruiting patients to participate in the study. If this occurs, many aspects of the design can be tested with healthy subjects, which are much easier to recruit.

Revised Schedule

Task Name	Duration	Start	Finish	Predecessors
Design Revisional Prototype	28 days	Thu 2/23/17	Mon 4/3/17	
Fabricate Revisional Prototype	19 days	Tue 4/4/17	Fri 4/28/17	1
IRB Approval	11 days	Mon 5/1/17	Mon 5/15/17	2
CES Approval Stamp for Revisional Prototype	6 days	Mon 5/1/17	Mon 5/8/17	2
Get Patient Feedback for Revisional Prototype	66 days	Tue 5/16/17	Tue 8/15/17	4,3



References

[1] AliExpress. (n.d.). [Image of Push Buttons, Snap Fasteners]. Retrieved March 25, 2017.

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Q&A

Thank you for your time and attention!